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EXPLORATORY SYSTEMS CONTROL MODEL (ESM). MAINTENANCE MANUAL.(U)
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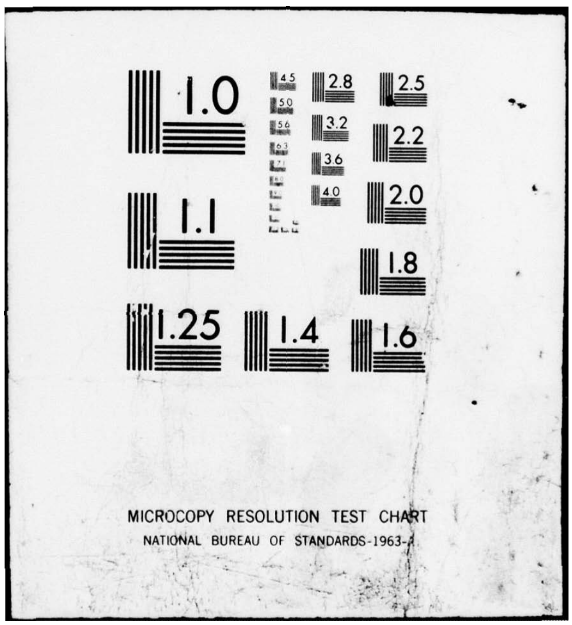
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(11) LEVEL II

APRIL 1977

MAINTENANCE MANUAL

EXPLORATORY SYSTEMS CONTROL MODEL (ESM)

for

THE DEFENSE COMMUNICATIONS AGENCY
WASHINGTON, D.C. 20305

Burroughs Corporation
Federal and Special Systems Group
Paoli, Pa. 19301

(18) SBIE

(19) AD-E100 145

(11) APRIL 1977

(9) Final rept. Jul 75-Apr 77,

(12) 225p.

Burroughs

MAINTENANCE MANUAL

(6)

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Maintenance Manual.

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DISTRIBUTION STATEMENT A
Approved for public release;
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Burroughs Corporation
Federal and Special Systems Group
Paoli, Pa. 19301

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FOREWORD

This publication is the Hardware Maintenance Manual for the Exploratory Systems Control Model (ESM). It provides the information needed for maintenance of all hardware items contained in ESM cabinets numbers 1, 2, and 3. This manual was prepared by Burroughs Corporation and is submitted in accordance with the requirements of contract DCA 100-75-C-0054.

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SECTION 1

INTRODUCTION

1.1 PURPOSE

This document provides the information needed for maintenance of all items contained in the ESM cabinets, numbers 1, 3, and 3, as described in Section 2. It does not, however, provide information required for the maintenance of other ESM items connected to these cabinets. That is, it does not cover maintenance of the Burroughs TD 802 Terminals. Similarly, it does not cover maintenance of the PDP-11/40 Host processors. These items are documented separately.

1.2 MAINTENANCE PHILOSOPHY

The maintenance concept applied to the ESM cabinets, described in Section 2, consists of two levels; (1) the first level deals with replacing a failed board or module, and (2) the second phase deals with repair of that failed board or module.

The first level can effectively be accomplished by operator or user personnel who are familiar with the ESM to the extent described in the ESM User Manual. The details of this level of maintenance are therefore contained within the User Manual, but are also repeated in Section 4 to provide completeness of this manual.

The second level of maintenance requires more detailed knowledge of the ESM. That knowledge is obtainable from the detailed descriptions, board schematics and layouts, intra- and inter-cabinet cable details, power distribution details, and backplane wiring details contained in Section 5 and Appendix A of this manual.

1.3 MANUAL ORGANIZATION

The remainder of this manual is organized in the following order:

SECTION 2 - Physical Configuration

This section briefly describes the overall ESM configuration of rings, host processors and terminals, and specifically defines the physical configuration of the ESM cabinets.

SECTION 3 - Theory of Operation

This section presents a general theory of operation of the nodal hardware. It also describes the mechanism for loading the ESM processor control memories from the Host Processor.

Additional detailed theory of operation is contained in paragraph 5.2 for the hardware, and in the Software Maintenance Manual for the software.

SECTION 4 - User Level Maintenance

This section describes the maintenance and diagnostics which may be performed by user personnel. It is extracted from the User Manual and reproduced herein. This section should be reviewed prior to attempting the Board Level Maintenance defined in Section 5.

SECTION 5 - Board Level Maintenance

This section provides the logic schematics, board layouts, and theory of operation for each PC Board. It also includes power supply and power distribution, inter- and intra-cabinet cables and cabinet components.

APPENDIX A - Backplane Wiring Details

This section provides the detailed backplane wiring lists.

1.4 RELATED DOCUMENTS

Other documents providing detailed information on the ESM are:

1. User Manual for ESM
2. Software Maintenance Manual for ESM
3. TD 700/800 Equipment Reference Manual
4. TD 802 Drawing Package

SECTION 2

PHYSICAL CONFIGURATION

2.1 ESM PHYSICAL CONFIGURATION

The ESM consists of the major physical entities shown on Figure 2-1. These include:

- 3 ESM Loops, or rings, each housed in a separate cabinet
- 2 CRT Terminals, Burroughs TD 802's
- 2 Host Porcessors, PDP-11/40's
- 1 set of interconnecting cables.

Additional system information is provided in the User Manual for the ESM.

Each of the three loops is contained in a separate cabinet. These cabinets are standard Burroughs B 711-2 completely enclosed cabinets, equipped with backplanes and cooling fans. The backplanes are located in the upper half of the cabinet and provide mounting and interconnecting capability for a total of 90 printed circuit boards arranged in two rows of 45 each. The cabinets are configured to provide for two nodes in the top row and two nodes in the bottom row, with the loop interconnections accomplished on the backplane. Each node consists of 14 PC boards. In addition, two PC boards are required for clock generation and retiming, and two others are required for program loading. Hence, a total of 60 slots are occupied in a completely equipped cabinet (e.g., cabinet number 2). Cabinet number 1 is equipped with only three nodes. Cabinet number 3 is fully equipped, except for a Host Interface Board. In addition, each node is provided with two slots wired to accommodate a plug-in monitor equipped with lights and switches. The monitor provides for manual operation and control of the B7* microprocessors, and facilitates fault verification and isolation procedures. (See Figures 2-2 and 2-3 for typical ESM cabinet characteristics.)

A power supply is located in the bottom of each cabinet. It has the capacity (75A at 5V) for supporting all logic contained in the cabinet and has adequate margin (4 nodes presently require only 45A) for supporting logic which could be added to the cabinet.

A row of cable connectors is also included as part of the backplane, below the two rows of PC boards. Up to 18 cables could be accommodated, although only 4 are required for ESM interconnections. All backplane connections (both PC boards and cable connectors) are wire wrap type, permitting easy reconfiguration of cabinet wiring.

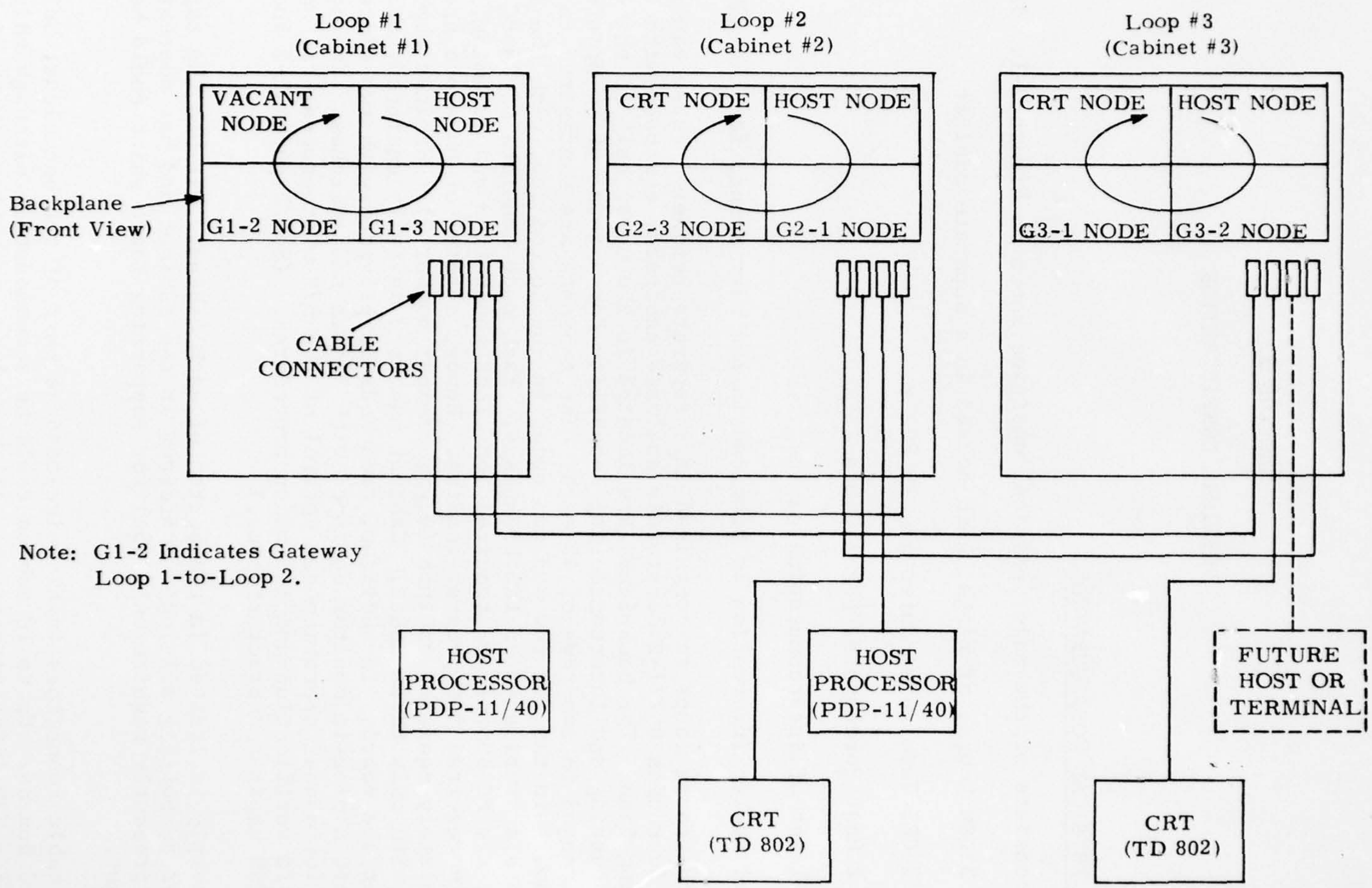


Figure 2-1. ESM Loops (Cabinets)

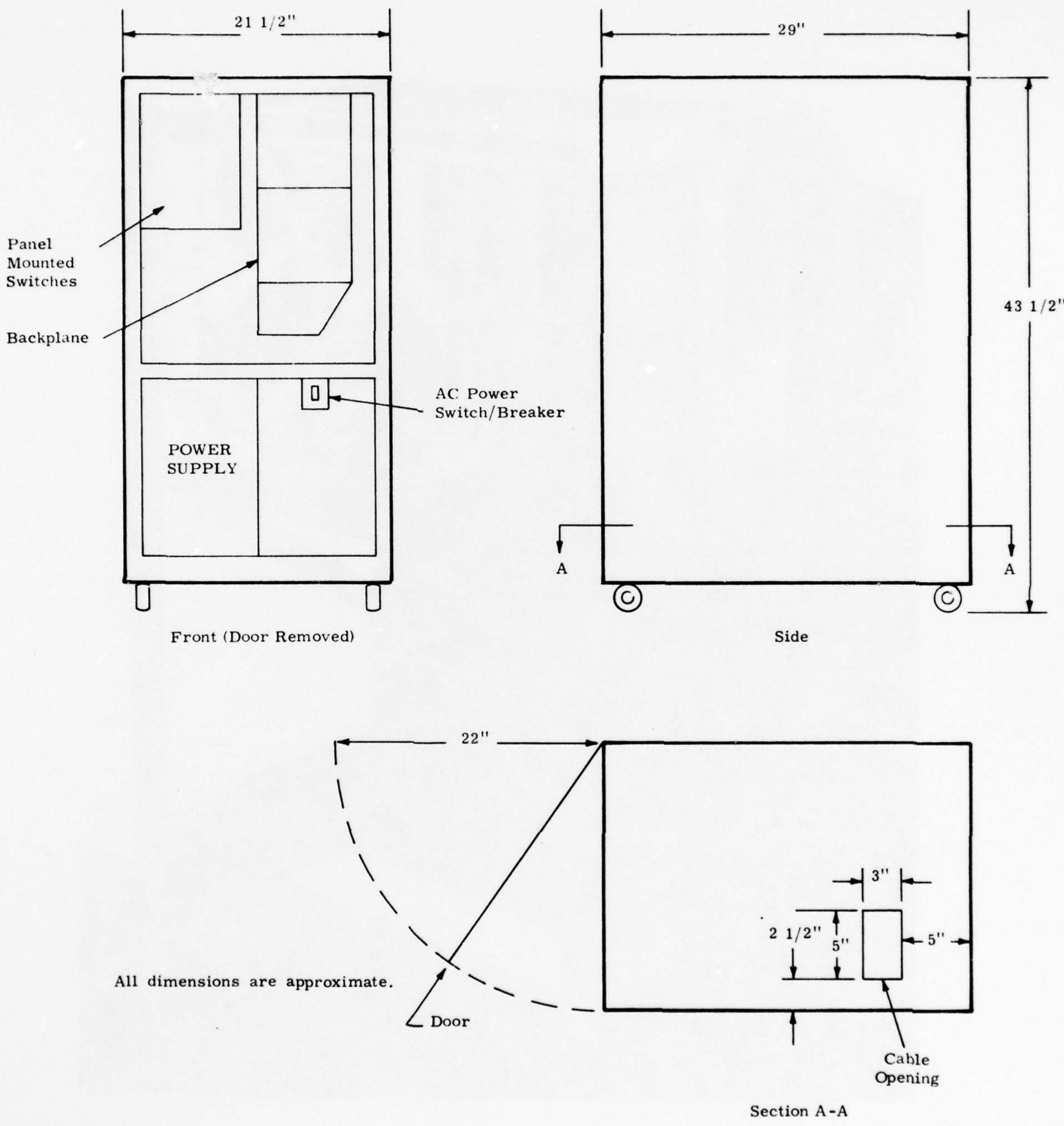


Figure 2-2. ESM Cabinet - Physical Characteristics

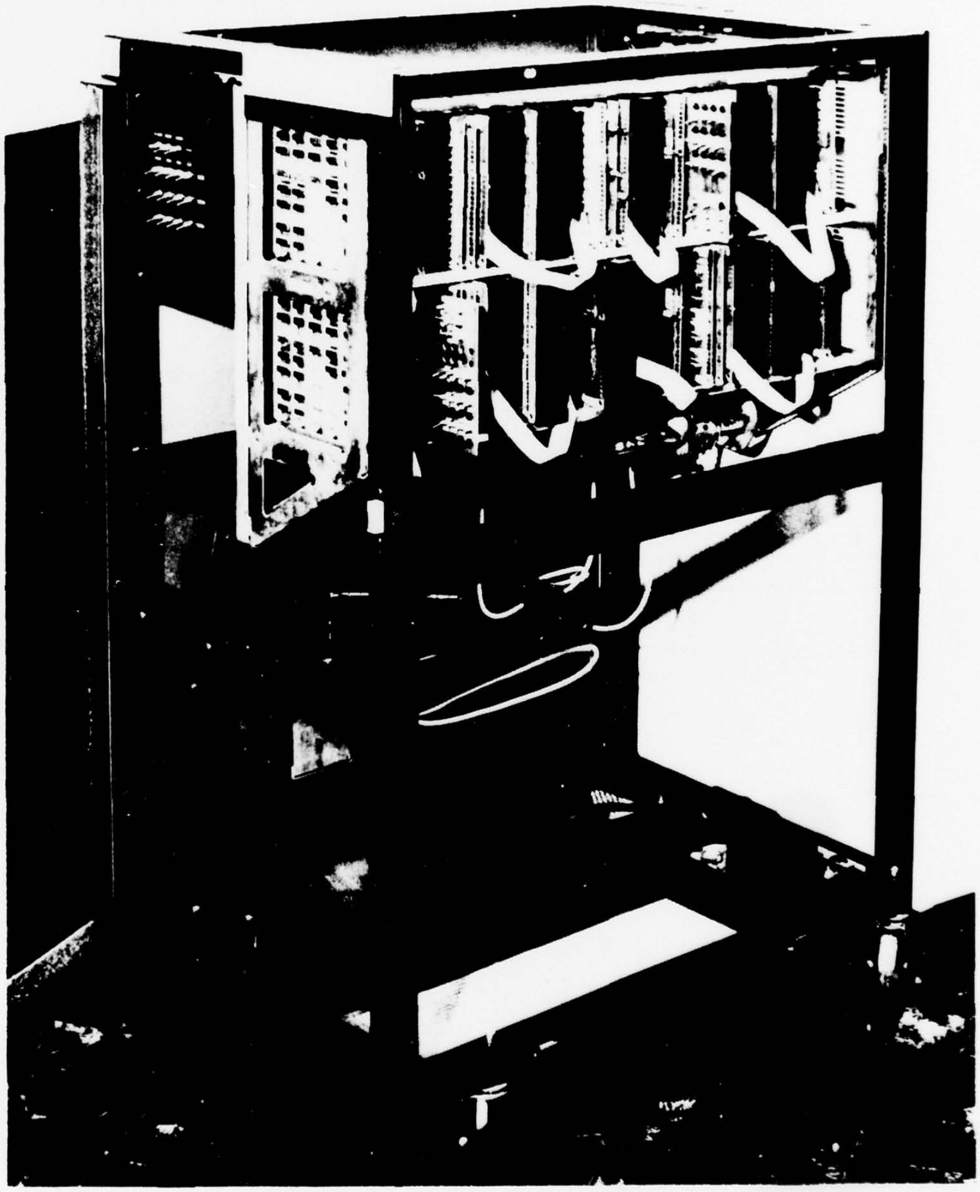


Figure 2-3. ESM Cabinet, Side Panels Removed

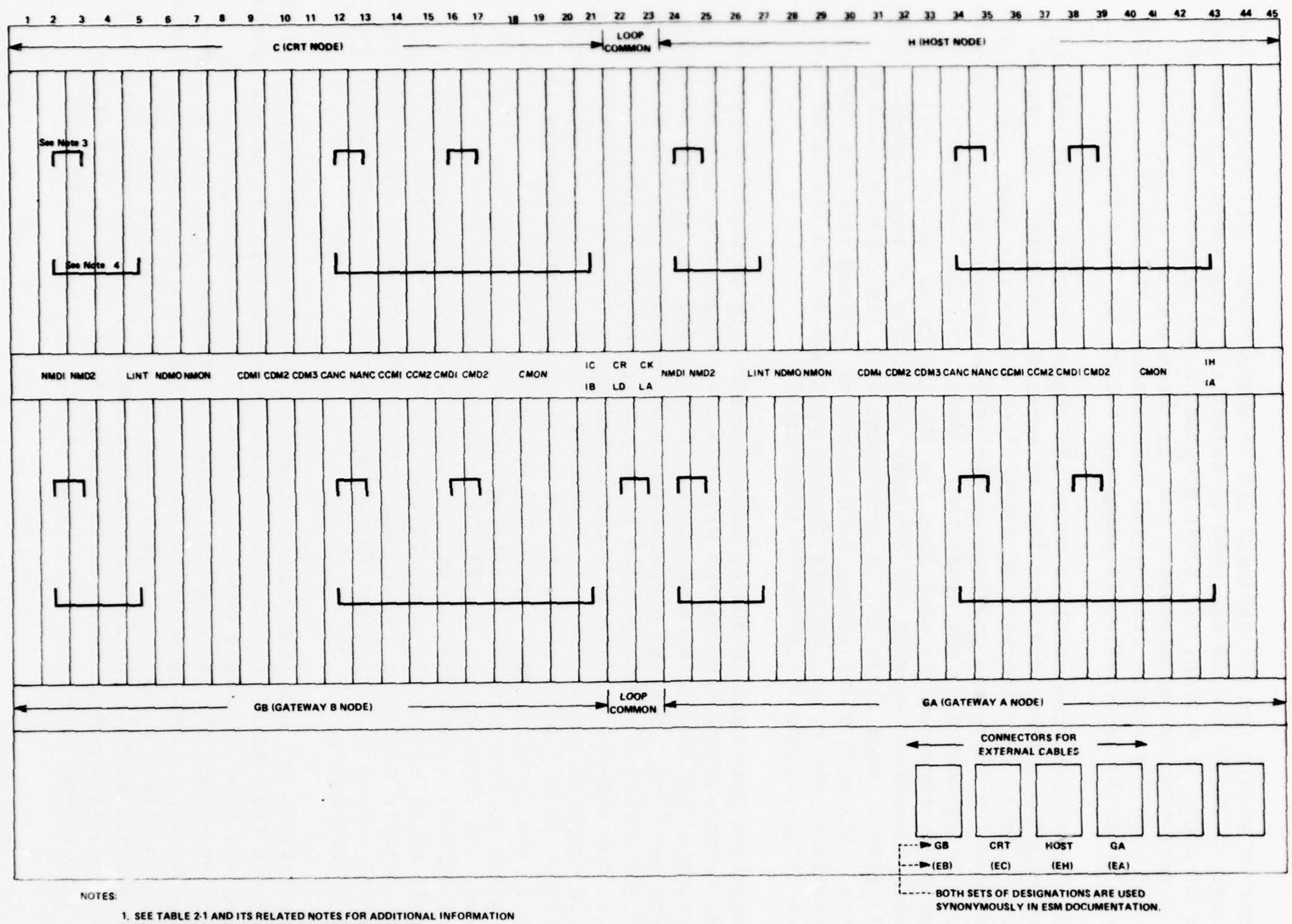
Figure 2-4 shows the actual location of the PC boards in the card slots of a cabinet. Table 2-1 provides a listing of all of these boards, and cross references pertinent information relating to them.

Operator's controls within the ESM cabinets are of three types: (1) Those mounted on the front edge of the PC boards and used to select the loop speed for each node and the number of nodes in a loop, (2) those mounted on the plug-in monitor and used for manual operation and maintenance, and (3) those mounted on the switch control panel and used for system loading and maintenance. The specific location and use of these controls is detailed in paragraph 4.1 of the User Manual.

As indicated in Figure 2-1, the complete nodes and their interconnecting cabling, which together comprise a loop, are contained in separate cabinets. The arrows on each cabinet indicate the direction of signal flow around the loop. The interconnections between the loops are provided by the cables between pairs of cabinets. Hence, each loop is connected to the other two. Similarly, the Host Processors and CRT terminals are connected to each loop via the indicated cables. All cables are equipped with connectors at each end for easy connection or replacement. Each connector is labeled at each cable end to correspond with its cabinet mounted mating connector. All cables are either flat ribbon or twisted pair and, except for the CRT terminals, enter the cabinets through openings in the bottom of the cabinet. Under-floor routing of cables is anticipated.

The CRT terminals are Burroughs TD 802's, each equipped with keyboard as well as display. These terminals can communicate with the Host Processors, as well as with each other, via the loop interconnections. Each TD 802 can display 24 lines of 80 characters per line. Message preparation is accomplished off-line by typing a message into the terminal's memory while it is simultaneously displayed on the CRT. Editing of the entered message is accomplished prior to transmission. Editing features include complete cursor control, character insert and delete, backspace, tabulate, and forms mode. After completion of editing, the entire message is transmitted in 3-line packet format (up to 256 characters per packet). Positive indication is given to the operator signifying successful transmission. Data is transmitted from, and received by, the TD 802 in an asynchronous mode at a transmission rate of 9600 bits (960 characters) per second. Impending-receipt of a message is signified by an audible alarm if the TD 802 is in the off-line (local) state. Further details regarding operation of the TD 802 are provided in Section 4 of the User Manual and in the Burroughs TD 700/800 Equipment Reference Manual supplied with the TD 802 units.

The ESM Host Processors are GFE (Government Furnished Equipment) and are configured as indicated in the User Manual for the ESM. These processors interface with their respective loops via Host Interface nodes per Figure 2-1. Data is transferred between the Host Processor and its respective node in bit-serial form at a transmission rate of 560 Kbps. Messages are formatted in 128 word (16 bits each) packets for transmission in either direction. Actual interface between the PDP-11/40 UNIBUS and the 560 KHz serial line is achieved via a DEC M1710 Universal Interface Module which was modified and is referred to herein as the Universal Interface Board (UIB). This ESM-supplied board was added to each of the two GFE Host Processors.



NOTES:

1. SEE TABLE 2-1 AND ITS RELATED NOTES FOR ADDITIONAL INFORMATION
2. SEE FIGURE 2-1 FOR CABLE CONNECTION INFORMATION.
3. FRONT PLANE CONNECTORS ARE USED TO INTERCONNECT THE FRONT EDGES OF ADJACENT P.C. BOARDS AS INDICATED BY THE SYMBOL ⊓.
4. FLAT RIBBON CABLES ARE USED FOR ADDITIONAL INTERCONNECTIONS BETWEEN P.C. BOARDS THAT ARE NOT ADJACENT. THESE INTERCONNECTS ARE SHOWN BY THE SYMBOL ⊔.

Figure 2-4. PC Board Locations

Table 2-1. PC Board Identification

Slot No.	Slot Ident.	Card Ident.	Part No.	Description
1				Vacant
2	NMD1	MD1	2600-5538M	Part of NCU B7*
3	NMD2	MD2	2600-5561M	Part of NCU B7*
4				Vacant
5	LINT	LIU	LIU	Line Interface Unit
6	NDMO	MPB	2601-8929M2	NCU Data Memory (1K)
7	NMON	(See Note 10)		NCU Monitor Access
8				Vacant
9	CDM1	MPB	2601-8929	CIE Data Memory (1st 4K)
10	CDM2	MPB	2601-8929	CIE Data Memory (2nd 4K)
11	CDM3	MPB	2601-8929M1	CIE Data Memory (Last 3K)
12	CANC	CIE ANC	CIE ANC	CIE Ancillary Logic
13	NANC	NCU ANC	NCU ANC	NCU Ancillary Logic
14	CCM1	7PM	2601-1668M	CIE Control Memory (1st 2K)
15	CCM2	7PM	2601-1668M	CIE Control Memory (2nd 2K)
16	CMD1	MD1	2600-5538	Part of CIE B7*
17	CMD2	MD2	2600-5561M	Part of CIE B7*
18				Vacant
19	CMON	(See Note 10)		CIE Monitor Access
20				Vacant
21 Top	IC	CRT INTF	CRT INTF	Interface Logic, CRT
21 Bott	IB	G'WAY INTF	G'WAY INTF	Interface Logic, Gateway B
22 Top	CR	CR	CR	Loop Clock Retimer

B7* is the designation of the Burroughs Microprocessor used in the ESM described herein.

Table 2-1. PC Board Identification (Cont)

Slot No.	Slot Ident.	Card Ident.	Part No.	Description
22 Bott	LD	LDR	LDR	Loop Loader
23 Top	CK	CK GEN	CK GEN	Loop Clock Generator
23 Bott	LA	LDR ANC	LDR ANC	Loop Loader Ancillary
24	NMD1	MD1	2600-5538M	Part of NCU B7*
25	NMD2	MD2	2600-5561M	Part of NCU B7*
26				Vacant
27	LINT	LIU	LIU	Line Interface Unit
28	NDMO	MPB	2601-8929M2	NCU Data Memory (1K)
29	NMON	(See Note 10)		NCU Monitor Access
30				Vacant
31	CDM1	MPB	2601-8929	CIE Data Memory (1st 4K)
32	CDM2	MPB	2601-8929	CIE Data Memory (2nd 4K)
33	CDM3	MPB	2601-8929M1	CIE Data Memory (Last 3K)
34	CANC	CIE ANC	CIE ANC	CIE Ancillary Logic
35	NANC	NCU ANC	NCU ANC	NCU Ancillary Logic
36	CCM1	7PM	2601-1668M	CIE Control Memory (1st 2K)
37	CCM2	7PM	2601-1668M	CIE Control Memory (2nd 2K)
38	CMD1	MD1	2600-5538	Part of CIE B7*
39	CMD2	MD2	2600-5561M	Part of CIE B7*
40				Vacant
41	CMON	(See Note 10)		CIE Monitor Access
42				Vacant

B7* is the designation of the Burroughs Microprocessor used in the ESM described herein.

Table 2-1. PC Board Identification (Cont)

Slot No.	Slot Ident.	Card Ident.	Part No.	Description
43 Top	IH	HOST INTF	HOST INTF	Interface Logic, Host
43 Bott	IA	G'WAY INTF	G'WAY INTF	Interface Logic, Gateway A
44				Vacant
45				Vacant

Notes:

1. Slots 1 through 21 in the top row comprise the CRT Node, except for Cabinet Number 1 (Loop Number 1) in which these slots are entirely vacant.

2. Slots 22 and 23, in both rows, house boards common to the entire loop.

3. Slots 24 through 45 in the top row comprise the Host Node.

4. Slots 1 through 21 in the bottom row comprise the Gateway B Node.

5. Slots 24 through 45 in the bottom row comprise the Gateway A Node.

6. Slot 43 of the top row in cabinet number 3 (Loop Number 3) will be equipped with a Host or terminal interface board in the future, but is presently vacant.

7. Boards in slots 5, 22 top, 23 top and 27 are equipped with RATE SELECTION switches. The Board in slot 22 top is also equipped with an ODD/EVEN switch.

8. Gateway A (GA) and Gateway B (GB) are in certain instances referred to more specifically as follows:

	Loop Number 1	Loop Number 2	Loop Number 3
GA	G1-3	G2-1	G3-2
GB	G1-2	G2-3	G3-1

Note that G1-3 indicates Gateway from Loop Number 1 to Loop Number 3.

9. Only PC Boards having identical part numbers are interchangeable. The letter M after a part number indicates a modification to the basic part number.

10. The ESM monitor described in Paragraph 4.1.4 of the User Manual is plugged into any monitor access slot (slots 7, 19, 29, and 41 of either row) as desired. The monitor is normally removed from the system during regular system operation. Part No. and card Identification for the ESM Monitor are "MON".

SECTION 3

GENERAL THEORY OF OPERATION

This section provides the general theory of operation of the ESM nodal hardware. A detailed description on a PC Board basis is provided in Section 5 of this manual. The associated software is defined in the Software Maintenance Manual for the ESM.

The nodal hardware illustrated in Figure 3-1, is configured around two Burroughs B7* microprocessors and, hence, can be described in terms of two processor-centered segments. The first segment consists of the Nodal Control Unit (NCU) microprocessor and its associated control memory, data memory, ancillary logic and loop interface logic. The primary purpose of this segment is to insert packets into the loop and to remove packets (containing an appropriate address) from the loop. Hence, it provides only for control and buffering relative to the communications loop.

The second segment consists of the Control and Interface Equipment (CIE) microprocessor and its associated control memory, data memory, ancillary logic, and external interface logic. This segment provides for overall node control, packet and message handling, traffic control and external device interfacing.

In addition to the nodal hardware of Figure 3-1 a Clock Generator, a Clock-Retimer and Loading Logic are required for each loop. The specific functions and characteristics of these units and of the individual elements of the NCU and CIE segments are described in detail in the following paragraphs.

3.1 NCU SEGMENT

The Loop Interface element contains the necessary cable drivers and receivers for direct loop interface. It includes the circuitry for deriving clock from the data stream and for maintaining frame synchronization relative to the data stream. It contains an address register, loaded by the B7*, and associated comparison circuitry to permit recognition of a specific address in an address field on the loop. Upon address recognition, the information word is streamed directly into the NCU data memory, while being monitored by the B7* for an end-of-packet (EOP) character.

The Loop Interface logic operates from one of three selectable clock rates: (1) 960 kHz, (2) 280 kHz, and (3) 12 kHz. The logic is contained on a single printed circuit board (PCB).

The NCU Microprocessor provides for control of the Loop Interface logic and the NCU Data Memory. That is, it establishes the Read or Write mode of operation (relative to the loop), sets the Loop Interface address register for a Read operation or initiates output for a Write operation, controls addressing of the Data

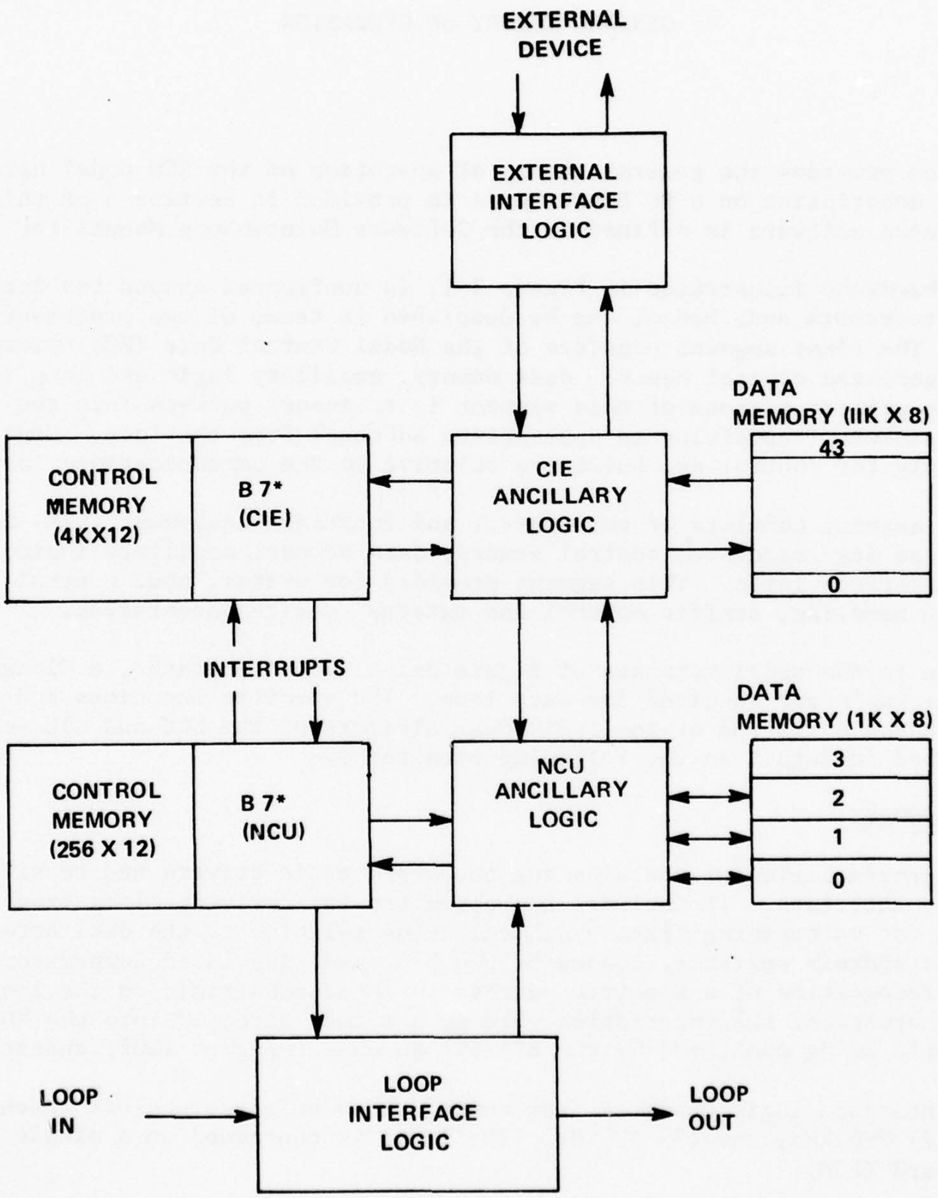


Figure 3-1. Node Configuration

Memory input and output locations and monitors the input/output stream for the EOP character. It interrupts the CIE microprocessor upon completion of the write/read cycle and responds to an interrupt from the CIE microprocessor to begin its next write/read cycle.

The NCU Microprocessor operates from the clock derived by the Loop Interface logic; hence, it operates in synchronism with the loop bit stream. Processor operation is bit-serial with 10 clocks (10.4 μsec) per instruction or per input/output byte (8 bits). The NCU microprocessor has 8-bit data registers, a 12-bit instruction register, and employs 8-bit memory addressing thereby permitting up to 256 words of control memory. This memory has 12-bit words and is provided in PROM form. The NCU microprocessor together with its control memory is contained on two PCB's.

The NCU Data Memory functions as I/O buffering relative to the loop and, in addition, provides a mailbox page for communication with the CIE microprocessor and for storing other loop control information. This RAM consists of 4 pages, each accommodating 256 8-bit words. It employs n-MOS semiconductor technology with a 350-nanosecond read or write cycle. It occupies one PCB.

The NCU Ancillary Logic provides for memory addressing and read/write control of the NCU Data Memory. That is, it provides NCU data memory access and control by both the NCU microprocessor and (when used with the CIE Ancillary Logic) the CIE microprocessor. It provides for serial/parallel data conversion to permit data transfer among the B7* (serial), Data Memory (parallel) and the communications loop (serial). It permits the routing of data to/from the microprocessor and several destinations (e.g., Data Memory or Loop Interface Logic). It permits direct memory-to-memory transfers between NCU and CIE Data Memories without processor handling, but under processor initiation. Finally, it contains a time-out clock that is read by the CIE Microprocessor and is used for such functions as reinitiating a write token or determining that a response has not been received within an allocated time period. The NCU Ancillary Logic is contained on one PCB.

3.2 CIE SEGMENT

The CIE Microprocessor provides for control of the entire node. It communicates with the NCU Microprocessor via interrupts and via the mailbox page of the NCU data memory. In this manner, it initiates NCU microprocessor operations relating to loop interfacing and it accesses NCU data memory I/O pages to transfer data between those pages and the I/O queues of its own data memory. As mentioned earlier, these inter-memory transfers are accomplished directly (memory-to-memory) in a parallel transfer mode. The CIE B7* determines message type (e.g., single address, multi-address, acknowledgement, etc.), does parity checking, generates ACK/NAK messages, determines alternate routing, controls I/O queues, does message assembly, loads/unloads buffers of the External Interface Logic, and maintains status of these buffers.

The CIE Microprocessor is very similar to the NCU microprocessor except that it operates from a 8.96 MHz clock with 9 clocks per instruction and employs 12-bit memory addressing, thereby permitting up to 4K words of control memory. This memory has 12-bit words and is in the form of external RAM on two PCB's. The CIE microprocessor (like the B7* NCU) is contained on two PCB's.

The CIE Data Memory primarily provides storage for assembling and queueing messages, in the form of packets, to/from the communications loop as well as to/from the external device. It also provides for storing user address and routing information, and includes work page capability. This RAM consists of 44 pages each accommodating 256 eight-bit words (i.e., a total of 11K words). It employs n-MOS semiconductor technology with a 350 nanosecond read or write cycle. It is contained on three PCB's.

The CIE Ancillary Logic provides for memory addressing and read/write control of the CIE Data Memory; together with the NCU Ancillary Logic it provides for access and control of the NCU Data Memory by the CIE Microprocessor. It also provides serial/parallel data conversion to permit data transfer among the CIE B7* (serial), Data Memory (parallel) and the External Interface Logic (parallel). It permits the routing of data to/form the microprocessor and several destinations (e.g., data memory, memory address register, interface logic, etc.). Finally, it permits direct memory-to-memory transfers between CIE and NCU data memories without processor handling, but under processor initiation. The CIE Ancillary Logic is contained on one PCB.

The External Interface Logic permits interface with an external host computer, an external CRT terminal, or another communications loop. It provides the necessary I/O buffers and controls to allow data transfer to/from the I/O queues of the CIE Data Memory and the external device (host computer, CRT terminal or communications loop). Data is transferred between data memory and the I/O buffers in the direct parallel transfer mode without processor handling, but upon processor initiation. Buffer status registers are set by the buffers and are read by the processor. Flags are set by the buffer and by the external device to control external data transfers in serial form. Necessary line drivers are included in the External Interface Logic.

This logic is contained on one PCB for each type of external device.

3.3 CLOCK GENERATOR

The clock generator develops the various clock signals required for the proper operation of the loop and its interconnected nodes. It consists of two separate crystal oscillators and the associated divider and driver logic to derive and output the necessary clock signals. The primary clock signals developed and their uses are:

Clock Signal	Function
8.96 MHz	CIE clock
1.92 MHz 560 KHz 24 KHz	NCU and Loop clock (one rate per loop, selected by card-mounted switches, and divided by two by CR)
560 KHz	Host Interface clock and Gateway Interface clock
96 KHz 9600 Hz	CRT Interface clock

Clock Signal	Function
96 KHz 2.8 KHz 1.2 KHz	Real time clock for CIE (one rate per loop selected by card-mounted switches).

Other logic clocks are also generated and distributed to the PCB's of each node.

3.4 CLOCK-RETIMER

A clock-retimer is provided for each communications loop. It accepts the loop clock signal from the clock generator and establishes the previously described loop frame format. It also accepts the data signal from the loop and provides data regeneration and data resynchronization, thereby compensating for effects relative to signal degradation and propagation time. This logic is contained on one PCB.

3.5 LOADING LOGIC

The Loader Board and the Loader Ancillary Board together provide the capability to load the CIE control memories of each of the ESM nodes. These boards accept serial data (and associated clock) from the Host PDP-11/40 that is connected to ESM Loop Number 2. This data, at 560 KBps, is routed to the appropriate control memory as a result of proper setting of the panel-mounted switches (on each cabinet) that are used for loading.

SECTION 4

USER LEVEL MAINTENANCE

The maintenance and diagnostics described in this section are those which may be performed by user personnel. However, it is assumed that these personnel are familiar with the ESM to the extent described in the User Manual. These maintenance activities include:

1. Cleaning of filters,
2. Replacement of fuses,
3. Verification of proper operation via successful running of diagnostics,
4. Isolation of faulty PC Boards via running of diagnostics, and
5. Replacement of an identified faulty board by a spare PC board.

Maintenance operations will require the removal of one or both side panels. These are lift-off panels, but panel retainer bolts at the bottom of the cabinet must first be loosened sufficiently to permit panel removal.

CAUTION

> When performing maintenance on an ESM cabinet, care must be exercised to insure that foreign matter does not fall into the cabinet power supply through the fan or other openings in the top of the power supply. This can best be accomplished by covering these openings when the fan is not operating (i.e., ac power is removed from the cabinet).

4.1 FILTERS AND FANS

Two filters are located in the bottom of each ESM cabinet. These filters are removed by rotating the retainer bar under the filter, tilting the filter and dropping it through the bottom of the cabinet. They should be removed and washed periodically (at least annually).

Fans are mounted at the upper rear of the cabinet and on the top of the cabinet power supply. These fans require no specific maintenance, but should be checked periodically for proper operation. Excessive noise or vibration would indicate a need for fan replacement or retightening of mounting hardware.

4.2 FUSE REPLACEMENT AND POWER SUPPLY CHECKS

Fuses can be replaced readily, but repeated failures can be attributed to more serious faults. Fuses of only the correct size and rating should be used. Fuse sizes and locations are presented in Table 4-1.

Power supply voltages should be checked periodically (at least semiannually). These checks should be made on both the backplane and the power supply itself. They include voltage level, ripple, and also balance between both halves of the backplane. Details of these measurements and any adjustments required are provided in paragraph 5.3 of this manual.

4.3 VERIFICATION OF PROPER OPERATION

Proper operation of the ESM hardware can be verified by running the diagnostic programs described in paragraph 4.6. That is, if all of the diagnostic routines run successfully, the hardware generally can be assumed to be good. Note, however, that these routines do not check every single function and, therefore, are not totally conclusive. But, they do provide a significant level of confidence of system operability.

4.4 ISOLATION OF FAULTY PC BOARDS

The existence of a fault in the ESM generally can be located by running the Diagnostics as described in paragraph 4.6. That is, the fault can be isolated to a Terminal, a Host, or one or more PC boards in any of the ESM cabinets. The suspected element can then be further verified by substituting a good element for the suspected element. For example, one CRT terminal can be substituted for another by moving the cable connector at the CRT end. Also, a spare PC Board may be substituted for a suspected faulty board in any of the three ESM cabinets, see paragraph 4.5, and after substitution the diagnostic(s) can be rerun to verify proper operation.

Table 4-1. Fuse Sizes and Locations

a. Two 30A, 32V, 5AG Fuses. Each fuse distributes 5V power to one half of the backplane. These fuses are mounted at the top rear of the power supply.

NOTE

Cabinet 1 uses one 30A fuse and one 15A fuse. The 15A fuse is for the left half (partially equipped) of the backplane.

b. Two 1/2 A, 125V, 3AG Fuses. One is used to protect the ac input of the cabinet fans; the other is used to protect the ac input of the power supply fan. These are in-line fuses.

c. One 2A, 250V, 3AG Fuse. Protects the +12V output (presently unused) of the power supply, mounted at the top front of the power supply.

d. One 3/4 A, 250V, 3AG Fuse. Protects the -12V output (presently unused) of the power supply, mounted at the top front of the power supply.

4.5 REPLACEMENT OF A FAULTY PC BOARD

Replacement of PC Boards is limited to those contained in the three ESM cabinets. A suspected faulty board in any of these cabinets can be replaced by a spare board of the same type, or by a board currently not being used in one of the other cabinets. As a precaution relative to accidentally causing an instruction to be changed in CIE Control Memory, the associated node should be placed in the DNEX state while removing or inserting a PC Board. For PC Board locations and complete identifications, refer to Figure 2-4 and Table 2-1, respectively.

4.6 LOADING AND RUNNING DIAGNOSTICS

This paragraph presents the procedures for loading and running the diagnostic programs supplied with the ESM. Those programs provide the capability to verify proper operation of the ESM or to verify that a fault exists. They also permit isolation of a fault to a specific hardware element, refer to paragraph 4.4. The flow charts and code listings for these programs are provided in the Software Maintenance Manual and should be referred to for a thorough understanding of the use and capabilities of these programs.

The procedure for loading the diagnostic(s) is as follows:

1. Mount Diagnostic Tape on Tape Transport of Host Processor B (connected to Loop 2).

2. At DECscope, do the following:

   - Set User Identification code to Access File by entering SET /UIC = [1, 4]

   - Move object file to disk. FLX DK0:/FB:256. = MT0: [1, 4] name. OBJ

   - Load object file into suspect node(s)' CIE's.

     RUN [20, 20] ESMLDR

     Enter filename.

3. At ESM cabinet:

   - Set LD/EN Switch to Up position

   - Set Selected Node LOAD Switch to Up position

   - Depress M-CLR pushbutton.

4. At DECscope: Press Carriage Return key to initiate loading.

NOTE

It is possible to load nodes in different loops simultaneously but not nodes within the same loop.

5. At appropriate ESM cabinet and node:

- Reset Node LOAD Switch (Switch Down)
- Reset LD/EN Switch (Switch Down)
- Run diagnostic using ESM Monitor.

NOTE

When loading with Monitor plugged-in, the Monitor should be in the RUN mode with RUN light on. (See paragraph 4.1.4 of User Manual.)

4.7 DESCRIPTION OF DIAGNOSTIC PROGRAMS

The following paragraphs identify the various diagnostic programs and describe their application to the ESM:

4.7.1 MEMORY CHECKING PROGRAM

Source file MEMCK.DAT

Object file MEMCKO.OBJ

Purpose: For checking NCU and CIE data memory boards.

Description: The bit patterns 10101010, 01010101 and sequential numbers are written into memory and read out again for all NCU and CIE memory pages. If all checks pass the program hangs at location NOERR. If there is an error in the NCU data memory the program hangs at NCUERR. If there is an error in the CIE data memory the program hangs at CIEERR. The operator may then single step the program to find the word and page number where the test failed and examine the contents of the bad page. There are a total of 44 CIE pages, 16 each on the first two CIE memory cards and 12 on the third card. Thus, a failure on page 16 would indicate a problem on the second data memory card. Pages are numbered 0 through 43.

4.7.2 BLOCK TRANSFER DIAGNOSTIC

Source file BLKS.DAT

Object file BLOUT.OBJ

Purpose: For checking memory reading and writing and block transfers between NCU and CIE Ancillary Boards.

Description: This program loads page 0 of the NCU with sequential numbers, reads them from the CIE and then block transfers page 0 of the NCU to page 3 of the CIE. The result of the transfer is then read and the program hangs at location NG1 on failure to read sequential numbers. The program then loads CIE page 6 with sequential numbers, reads the data and then block transfers to page 2 of the NCU. The result of the transfer is then read and the program hangs at location NG2 on failure. The program hangs at HANG5 if there are no failures.

Special Instructions: The NCU must be in a "DON'T EXECUTE" state so that it may not modify its data memory.

4.7.3 GATEWAY DEBUG DIAGNOSTIC

Source file GTB.DAT

Object file GTBO.OBJ

Purpose: To check gateway interfaces between two cabinets.

Description: The program is loaded into gateway nodes in two loops. One gateway sends sequential numbers to the other gateway which reads the result. The sending gateway loads CIE page 0 with sequential numbers, sends the page across the interface and then may read the original page, if required. The reading gateway code starts at octal location 40. It block transfers the output buffer contents to CIE page 1 and reads the results.

4.7.4 CRT-TO-CRT VIA GATEWAY DIAGNOSTIC

Source files	CTCC.DAT CTCG.DAT
Object files	CTCCO.OBJ CTCGO.OBJ

Purpose: For checking in loops No. 2, No. 3 gateway interface, partial loop (node) verification, and CRT interfaces.

Loading Instructions: Object file CTCCO.OBJ is loaded into CRT nodes on loops No. 2 and 3. Object file CTCGO.OBJ is loaded into gateway node GB in loop No. 2, and gateway node GA in loop No. 3. Put other nodes into DNEX and CLEAR state via panel-mounted switches while running diagnostic.

Description: These programs accept a packet from a CRT, send the packet via the loop to a gateway node, transfer the packet across the interface, and then deliver the packet to the CRT via the loop. After hitting the master clear and loop clear, acceptable operation allows a packet to be transmitted from one CRT to the other CRT connected to the other loop. Messages may be sent in either direction. A terminal that is in local mode will beep when there is a packet to be received.

4.7.5 CRT INTERFACE DIAGNOSTIC

Source file	CRTCK.DAT
Object file	CRTOBJ.OBJ

Purpose: For checking CRT interface boards and TD 802 CRT operation.

Description: This program accepts a packet from the CRT and then resends the packet back to the CRT preceded by 7 line feeds. The operator types a packet (up to 3 lines), transmits the packet and proper operation results in the packet being displayed on the bottom part of the screen.

4.7.6 PDP-11 INTERFACE DIAGNOSTIC

PDP-11 files:	Source PDP.FOR
	Object PDP.OBJ
	Task [1,4] PDP.TSK
CIE files:	Source PDP.DAT
	Object PDPO.OBJ

Loading: Load the PDP-11 connected CIE's with PDPO.OBJ. Run the CIE connected B7*. Run the task on the PDP-11 to be tested; i.e., RUN [1,4] PDP.TSK.

Purpose: This program checks the M1710 PDP-11 interface and the Host Interface Board. A three-line-packet is entered on the DECWRITER. The CIE hangs (at HNG1) after receiving the packet, and memory page 20 can be examined by single-stepping. The packet may then be written back to the DECWRITER by running the program from location WRTB.

4.7.7 LOOP CHECK DIAGNOSTIC

Source file LPCK.DAT

Object file LPCKO.OBJ

Purpose: For checking reading and writing ability of Loop Interface boards, loop operation, and Clock-Retimer operation.

Description: This program contains the code for writing a packet of sequential numbers to the loop and for reading the packet from the loop. For a successful read the program hangs at location NOERR. For an unsuccessful read the program hangs at location ERROR where the word location and data of the bad read can be examined.

Operating Procedures: For each loop, one node is designated the writer and one node the reader. For the writer, toggle in two STEP (hex 187) instructions at octal addresses 16 and 17. Put other two nodes into DON'T EXECUTE, CLEAR state. To run the test, clear the loop, clear the reader, and then clear the writer. The reader will then halt at location ERROR or NOERR depending on the outcome of the test.

SECTION 5

BOARD LEVEL MAINTENANCE

This section provides the detailed information required for Board level maintenance of the ESM. It includes logic schematics, board layouts and theory of operation for each of the PC Boards. These boards are all installed in the ESM cabinets, except for the Universal Interface Board (UIB) which is installed in each of the PDP-11/40 processors that are connected to the ESM loops.

The latter parts of this section also define the power supply and power distribution, the intra- and inter-cabinet cables, and the cabinet components. The Backplane wiring is presented in Appendix A.

5.1 GENERAL

All PC Boards used in the ESM cabinets are of the same physical size (6" x 6.5") but are equipped with varying quantities of chips, up to a maximum of 45 per board. Both plastic and ceramic chips are employed, but any ceramic chip may be replaced by its plastic equivalent. All chips except memory chips are of the TTL type. Memory chips are NMOS, but interface directly with the TTL chips. All chips, both TTL and NMOS require only one voltage, namely +5 volts. However, the CRT Interface Board provides an option for an EIA Interface with a compatible terminal and, as such, that option employs positive and negative 12 volts for EIA line interface levels.

All TTL chips are of the 74XXX Series, the 74HXXX Series, or the 74SXXX Series except for the EIA Interface chips which are MC 1488L and 1489L. Memory chips are 2102A's and 2606's. The former are used on the 7PM Boards and the MPB Boards. The latter are used as buffers on the Host Interface Board and the Gateway Interface Board. Finally, the PROMS employed on the NCU MD1 Boards are Harris HM-7611's.

All chips have either 14 pins or 16 pins and are installed in plug-in sockets. V_{cc} and ground pin assignments are as follows:

Chip Type	Gnd pin	V_{cc} Pin
14 Pin TTL	7	14
16 Pin TTL	8	16
16 Pin 2102A	9	10
16 Pin 2606	8	14

Chip Type	Gnd pin	V_{cc} Pin
16 Pin HM1-7611-5	8	16
14 Pin MC1488L	7	1=-12V, 14=+12V
14 Pin MC1489L	7	14
14 Pin 7490	10	5

Wherever one-shots are used on a board, the required output pulse durations are shown on the logic diagrams and are further described in the logic descriptions. It should be noted that capacitors are used with most of the one shots to establish pulse duration. Both fixed and variable capacitors are used, either alone or in combination. Generally, the fixed capacitors have a tolerance of ±10%. Hence, the capacitor values shown on the schematics are nominal values; when replaced, a value should be chosen to provide the desired pulse duration. It should also be noted that individual chips have varying values of internal capacitance and their replacement may also result in varying the output pulse duration. Finally, the capacitor values may change as a function of aging, hence the specified pulse durations should be checked periodically, or suspected if a board malfunction is detected.

5.2 PC BOARDS

This section provides a detailed description of each of the PC Boards. Each description includes logic description, logic schematic, parts layout and parts list. The PC Boards are presented here in the following order:

Para.	BOARD IDENT(S).	BOARD DESCRIPTION	Part Nos.
5.2.1	CK GEN	CLOCK GENERATOR	CK GEN
5.2.2	CR	CLOCK RETIMER	CR
5.2.3	MD1 & MD2	B7* MICROPROCESSOR (NCU & CIE)	2600-5538 & 5538M 2600-5561M
5.2.4	7PM	PROGRAM MEMORY	2601-1668M
5.2.5	MPB	DATA MEMORY	2601-8929, 8929M1 & 8929M2
5.2.6	NCU ANC	NCU ANCILLARY	NCU ANC
5.2.7	CIE ANC	CIE ANCILLARY	CIE ANC
5.2.8	LIU	LOOP INTERFACE UNIT	LIU
5.2.9	HOST INTF	HOST INTERFACE	HOST INTF
5.2.10	UIB	UNIVERSAL INTERFACE	UIB
5.2.11	G'WAY INTF	GATEWAY INTERFACE	G'WAY INTF
5.2.12	CRT/DTRM	CRT/DTRM INTERFACE	CRT INTF

Para.	BOARD IDENT(S).	BOARD DESCRIPTION	Part Nos.
5.2.13	LDR & LDR ANC	LOADER & LOADER ANCILLARY	LDR & LDR ANC
5.2.14	MON	MONITOR	MON

5.2.1 CLOCK GENERATOR BOARD

The Clock Generator Board develops the various clock signals required for operation of the loop and its connected nodes. All clock signals are derived from two separate crystal oscillators mounted on the board. A switch mounted on the front edge of the board is used to select one of three available loop-clock rates.

5.2.1.1 Clocks for CIE B7*'s, Host and Gateway Interfaces, and Loop

Refer to Figure 5-1, sheets 1 and 2 and figure 5-2 for the following logic discussion. Oscillator number 1 (OSC-1) provides an output frequency of 8.96 MHz. This frequency is buffered by four separate inverters and exits the board at Pins 1B, 1W, 1U and 1Y. These outputs are used by the CIE B7*'s as their input clock. The output of OSC-1 is also applied to a series of four flip-flops, each configured to divide its input by two. Thus, a 560 KHz symmetrical clock signal is derived and applied to pins 1, 3, 9, 11, and 13, of B7. These signals are buffered and routed as follows:

a. From Clock Generator Board terminal 1P to the Host Interface Board (Backplane slot 43 Top), 1N to Gateway Interface Board GB (Backplane slot 21 Bottom) and 1D to Gateway Interface Board GA (Backplane Slot 43 Bottom).

b. From Clock Generator Board terminal 1K to the UIB Board (Host M1710 Board) via Backplane connector EH and ESM-to-Host cable.

c. From inverter B7, pin 2, to pin F of switch S1. With the switch in MED position (Medium Loop Rate) this signal is routed from the Clock Generator Board terminal 1C to the Clock Retimer Board where it is used to establish the loop transmission rate. The output from switch S1 is also routed to C5, pin 11, as shown in Figure 5-1, sheet 2. Its use there is described in paragraph 5.2.1.3.

Oscillator number 2 (OSC-2) provides an output frequency of 7.68 MHz. This signal is divided by two series-connected flip-flops, each configured to divide by two. The resulting symmetrical 1.92 MHz clock signal is routed to another string of dividers, and to pin C of switch S1. With the switch in the HIGH position (High Loop Rate), this clock signal is routed to the Clock Retimer Board where it is used to establish the loop transmission rate. As indicated above, the output from switch S1 is also routed to C5, pin 11, as shown on Figure 5-1, sheet 2.

The 1.92 MHz signal is the input to pin 1 of C7. The output at pin 12 of C7 is a symmetrical signal of 192 KHz. This 192 KHz signal is divided by eight (three flip-flops) and applied to pin A of switch S1. It is also routed to E7, pin 2, as shown on Figure 5-1, sheet 2. With the switch in the LOW position (Low Loop Rate), this clock signal is routed to the Clock Retimer Board where it is used to establish the loop transmission rate. As indicated above, the output from switch S1 is also routed to C5, pin 11.

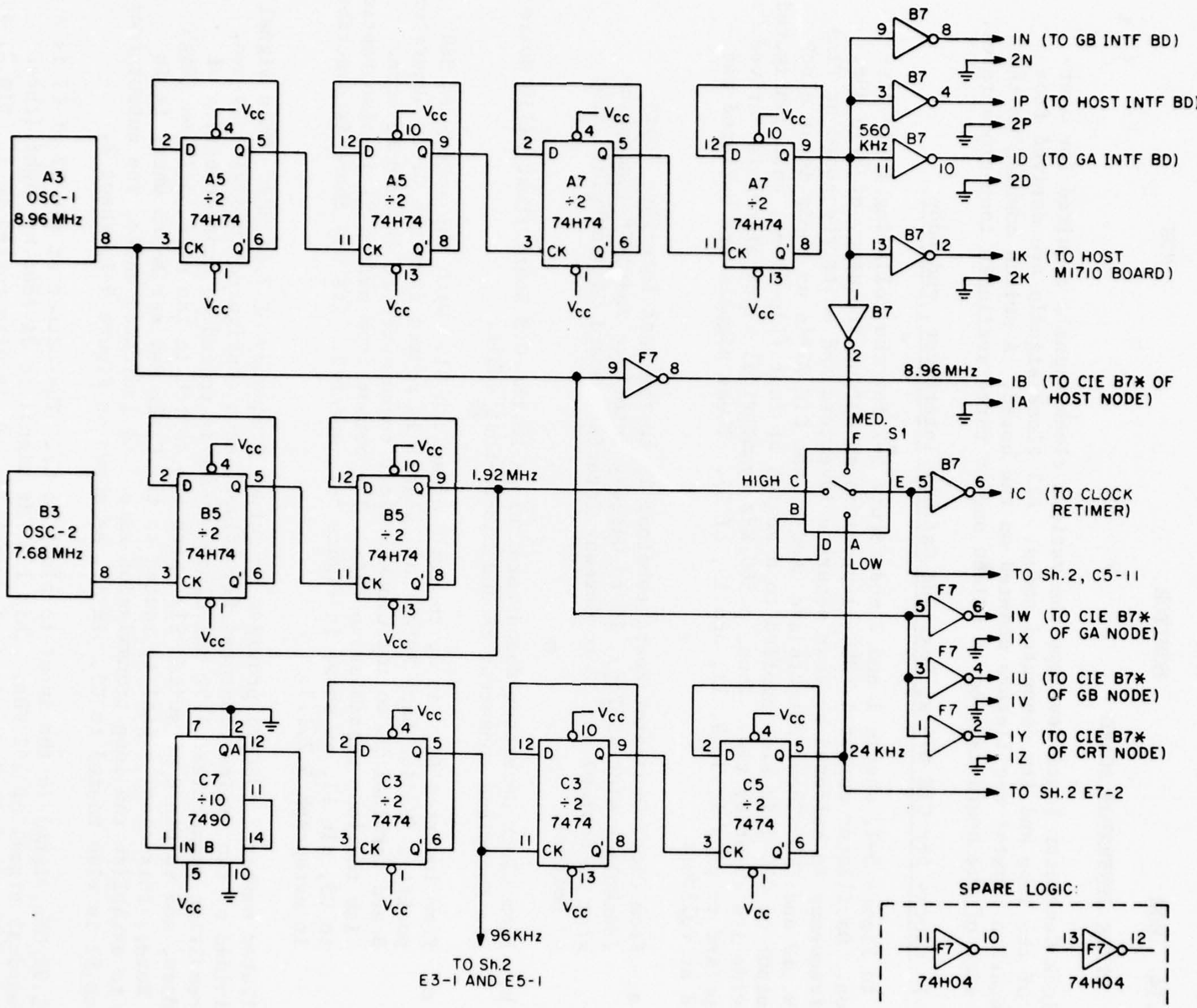


Figure 5-1. Clock Generator Board, Logic Diagram (Sheet 1 of 2)

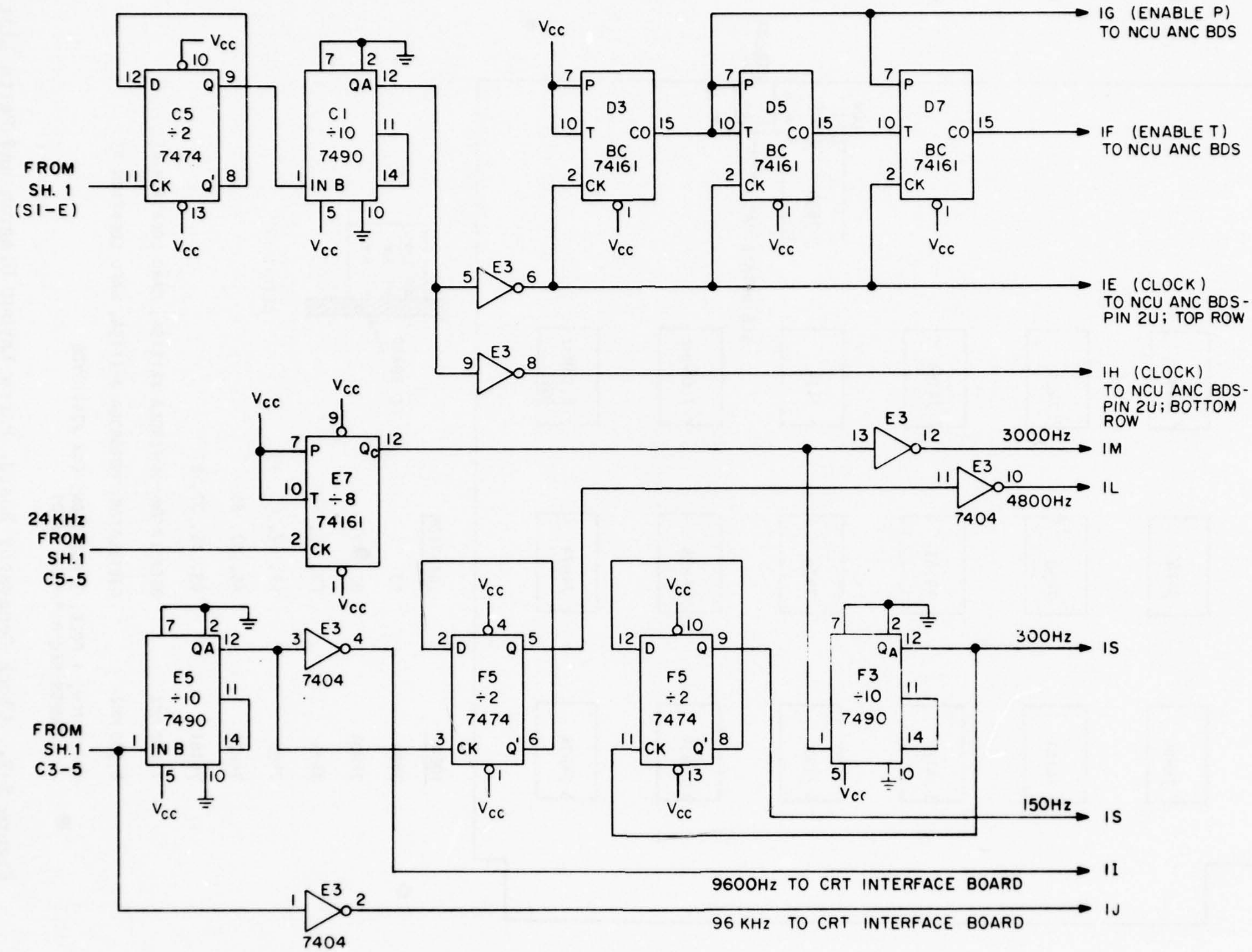
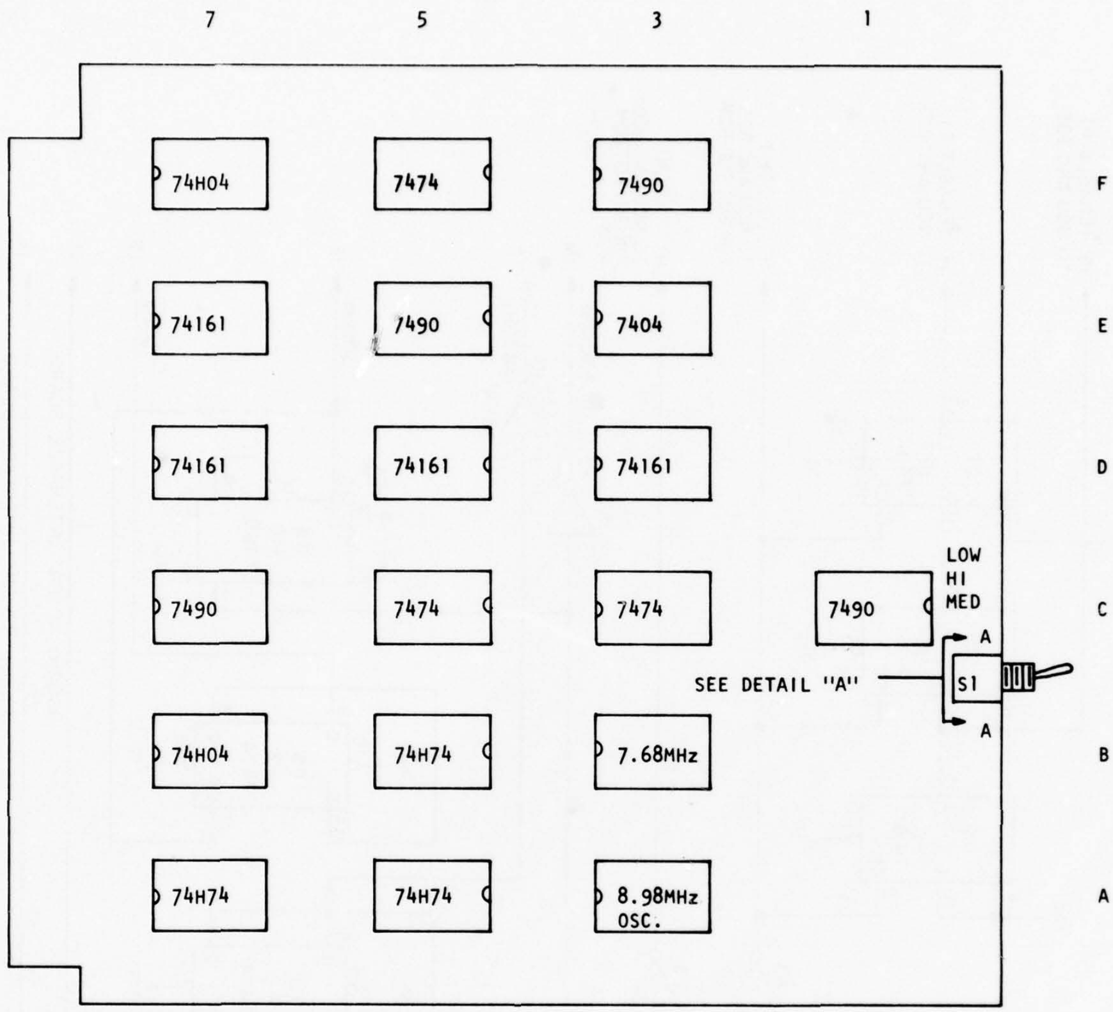
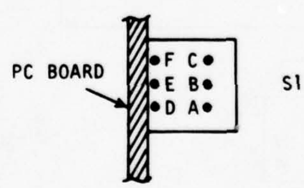


Figure 5-1. Clock Generator Board, Logic Diagram (Sheet 2 of 2)





DETAIL "A"

IDENT	LOCATION
7404	E3
74H04	B7, F7
7474	C3, C5, F5
7490	C1, C7, E5, F3
74H74	A5, A7, B5
74161	D3, D5, D7, E7
7.680 MHZ	OSCILLATOR, MOTOROLA #K1115A, CARD LOCATION B3
8.980 MHZ	OSCILLATOR, MOTOROLA #K1115A, CARD LOCATION A3

S1-SWITCH, 1 POLE, 3 POSITION, C&K #7411SYZQ
(JUMPER REQ'D PINS [illegible] to D)

Figure 5-2. Clock Generator Board, Parts Layout Diagram and Parts List

5.2.1.2 <u>Clocks for CRT Interface or Terminal Interface</u>

An intermediate output of 96 KHz is routed from C3, pin 5, (on Figure 5-1, sheet 1) to E3, pin 1, and E5, pin 1 (on sheet 2). The 96 KHz signal at E3, pin 1, is inverted (buffered) and fed out at Clock Generator Board terminal 1J. From there it goes to the CRT Interface Board in Backplane slot 21 Top.

The 96 KHz signal at E5, pin 1, is divided by ten, buffered by inverter E3, pins 3 and 4, and fed out as a 9600 Hz clock via terminal 1I. From there it also goes to the CRT Interface Board in Backplane slot 21 Top.

The 9600 Hz output at E5, pin 12, is also routed to F5, pin 3. This divide-by-two flip-flop produces a 4800 Hz signal which is buffered and fed out at terminal 1L. This signal is available for future use.

The 24 KHz signal from sheet 1 is divided by E7 and inverted to provide a symmetrical 3000 Hz output at 1M. From there it may be routed to the CRT Interface Board in slot 21 Top.

The 3000 Hz signal from pin 12 of E7 is divided by F3 to provide a symmetrical 300 Hz output at 1S. From there it may be routed to the CRT Interface Board.

It should be noted that the CRT Interface Board requires the 96 KHz and 9600 Hz clocks for operation with the TD 802 CRT Terminal. However, by using the 3000 Hz and 300 Hz clocks, it can operate with a 300 Bps data terminal; e.g., the TI Silent 700.

5.2.1.3 <u>Clocks for Time-Out Clock</u>

The upper half of Figure 5-1, sheet 2, details the logic required to generate clock signals which are required by the Time-Out clock logic located on the NCU Ancillary Boards. The input signal at pin 11 of C5 is one of three frequencies selected by the position of switch S1. The rates are:

HIGH	1.92 MHz
MEDIUM	560 KHz
LOW	24 KHz

This signal is divided first by two and then by ten, and applied to the inverters at pins 5 and 9 of E3. The outputs of these inverters exit the Clock Generator Board at terminals 1E and 1H. 1E provides clock signals to the Time Out clocks on the NCU Ancillary Boards in Backplane slots 13 Top and 35 Top. 1H provides the same for Backplane slots 13 Bottom and 35 Bottom.

The output from E3, pin 6, is also used to clock the series of divide-by-sixteen circuits (D3, D5 and D7). The resulting signals exit the Clock Generator Board at terminals 1G and 1F. These outputs go to the Time-Out clocks on the NCU Ancillary Boards in Backplane slots 13 Top and Bottom, and 35 Top and Bottom. The signal at terminal 1G has the duration of one clock cycle appearing at terminal 1E and a repetition rate of one-sixteenth of the frequency of the signal at 1E. The signal at terminal 1F also has the duration of one clock cycle appearing at terminal 1E, but a repetition rate equal to the frequency at 1E divided by 4096. Note that the signal at terminal 1E can be any of three rates as selected by switch S1.

5.2.2 CLOCK-RETIMER

The Clock-Retimer (CR) accepts a specific clock frequency at pin 1J (Figure 5-3, sheet 1, and Figure 5-4) from the Clock Generator Board and generates a specifically defined frame format for the loop. If the Clock-Retimer is in the Reset mode, determined by the up position of the panel mounted RESET switch, all zeros are inserted into both the address field and the data field of the newly generated frame. However, if the RESET switch is in the normal (down) position, the data received from the loop, at pin 2E, is reinserted into the newly generated frame format. Hence, the data received from the loop by the Clock-Retimer is retimed (reclocked) and regenerated for reinsertion on the loop at pin 2Q. In this manner cumulative degradations are removed from the loop upon each revolution of data around the loop.

The clock signal from the Clock Generator Board is applied to the Clock Retimer Board at pin 1J. This clock signal is a symmetrical square wave having TTL levels of 0 and 5V, and one of three selectable frequencies: 1.92 MHz, 560 KHz and 24 KHz. The Clock-Retimer Board is equipped with a three-position switch (S1), labeled HIGH, MED, LOW. This switch must be set to the proper position corresponding to the clock frequency being supplied from the Clock-Generator Board. That is, the switch on the Clock-Retimer Board must be set to the same position as the corresponding switch on the Clock-Generator Board. This switch selects the appropriate capacitors, see Figure 5-3, sheet 1, to establish the pulse widths for the one-shots of chip B1.

The Clock-Retimer Board is equipped with another switch (S2) labeled, ODD, EVEN. It is set to the position corresponding to the number of nodes in the loop that is employing the Clock-Retimer Board. In the ODD position it provides an additional 9 bits of delay, via flip-flop C3 and Shift Register D1, corresponding to a node in the loop. The effect is that the loop always appears to have an even number of nodes.

The following description is provided in two parts corresponding to the two modes of operation; namely "reset" and "normal", as selected by the panel-mounted RESET switch.

5.2.2.1 <u>Reset Mode</u>

In the reset mode, the panel-mounted RESET switch is in the "up" position resulting in the application of a ground to pin 2N of the CR board. This ground then appears at the "clear" input of the one shot, C1. Hence, the outputs of the one shot C1 are a continuous low at pin 13 and a continuous high at pin 4. The low from pin 13 results in highs at pins 10 and 13 of flip-flop C5, via the gates of C7, and a continuous low at the clock inputs of quad flip-flops D5 and E5. The high from pin 4 of C1 is applied to the preset input of flip-flop B3. Hence, in the RESET mode, the above identified flip-flops of B3 and C5 operate in the clocked mode only and the flip-flops of D5 and E5 are not clocked at all.

The clock signal from the Clock Generator board is applied to the CR board at pin 1J. As indicated earlier, this is a symmetrical square wave at one of three selectable frequencies. The discussion that follows, however, will deal specifically with the highest rate only, namely 1.92 MHz.

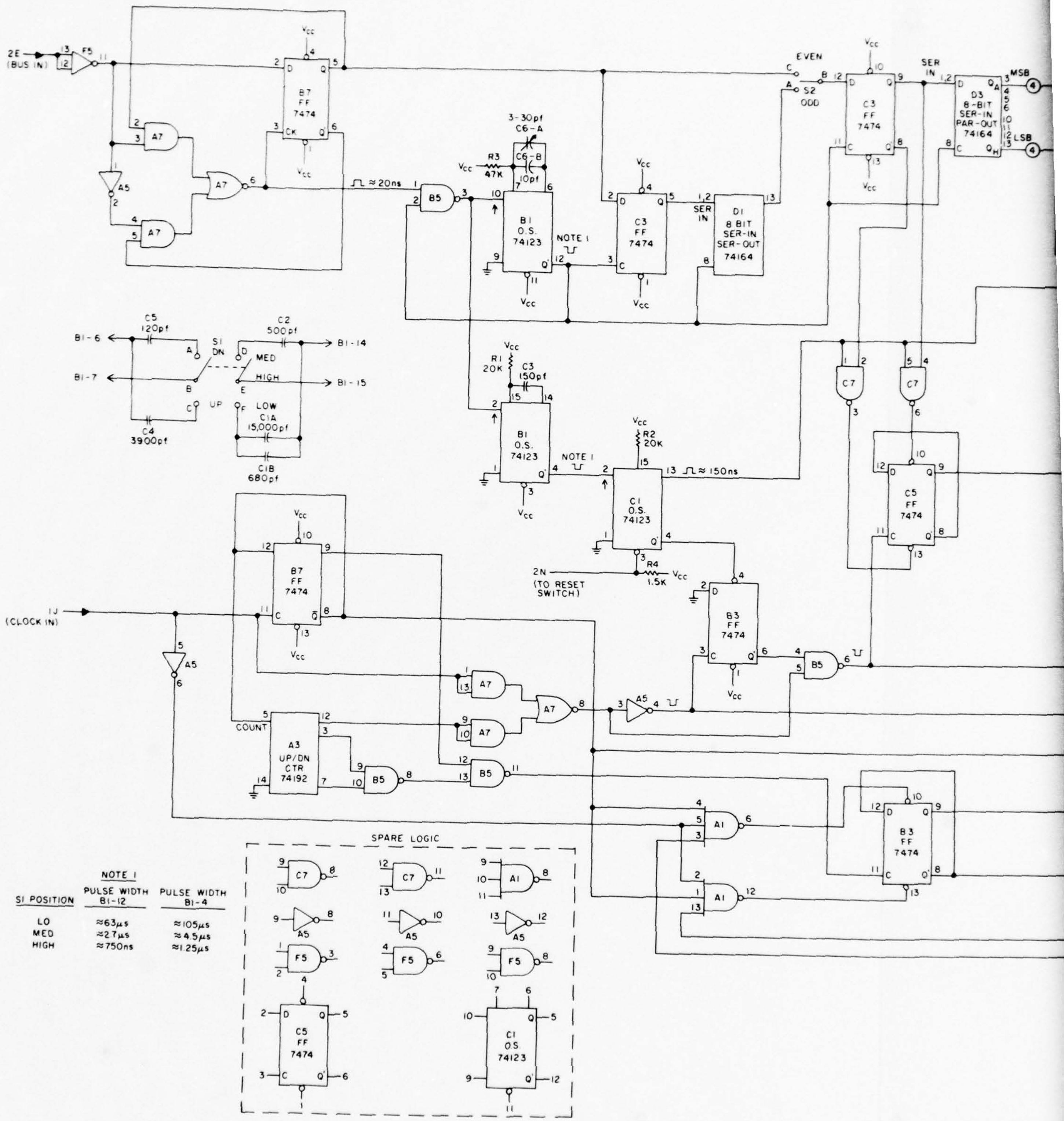
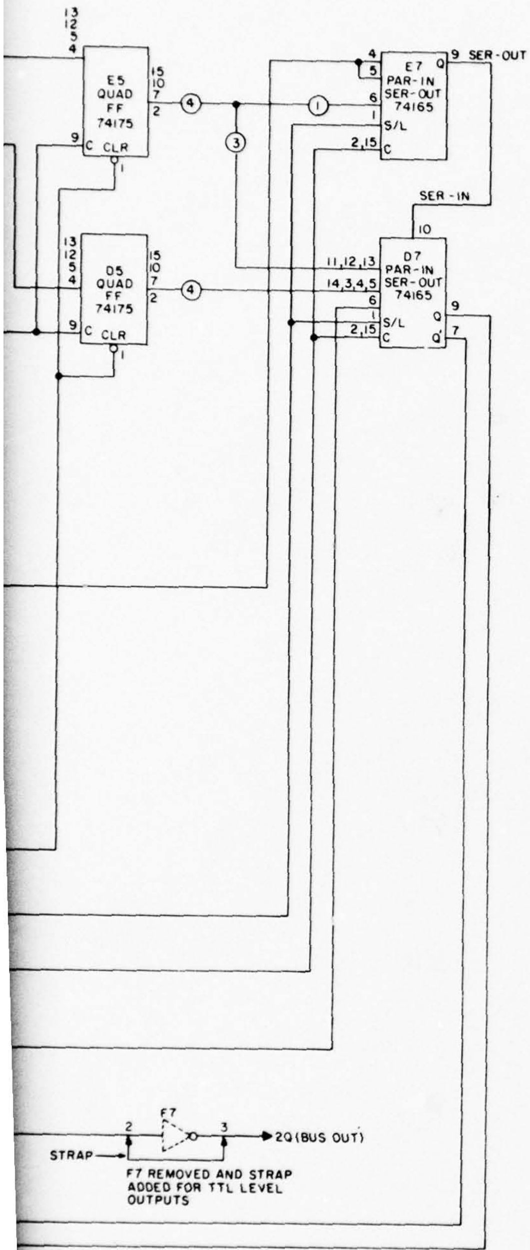


Figure 5-
Logic I



-3. Clock Retimer Board,
Diagram (Sheet 1 of 2)

2

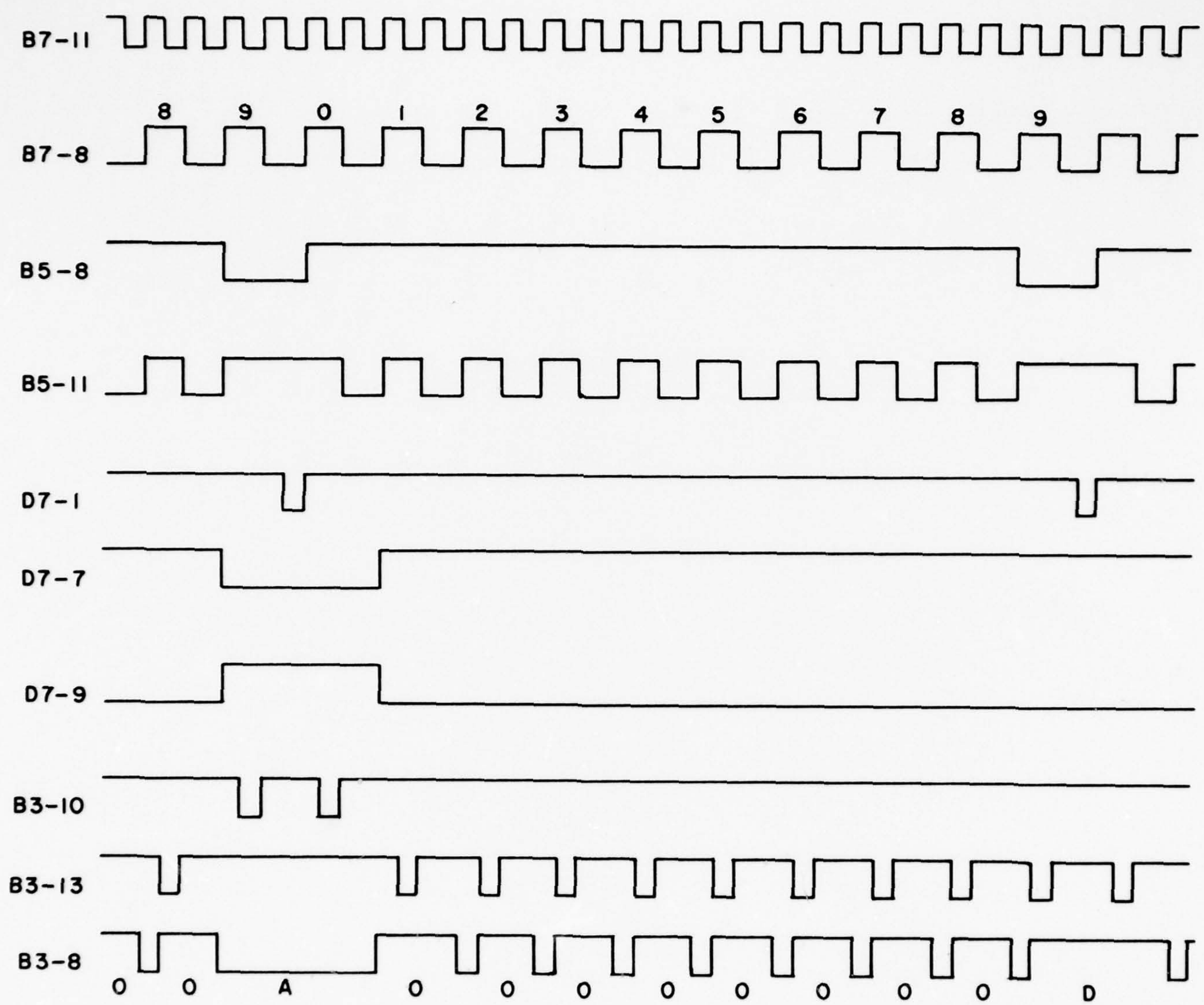
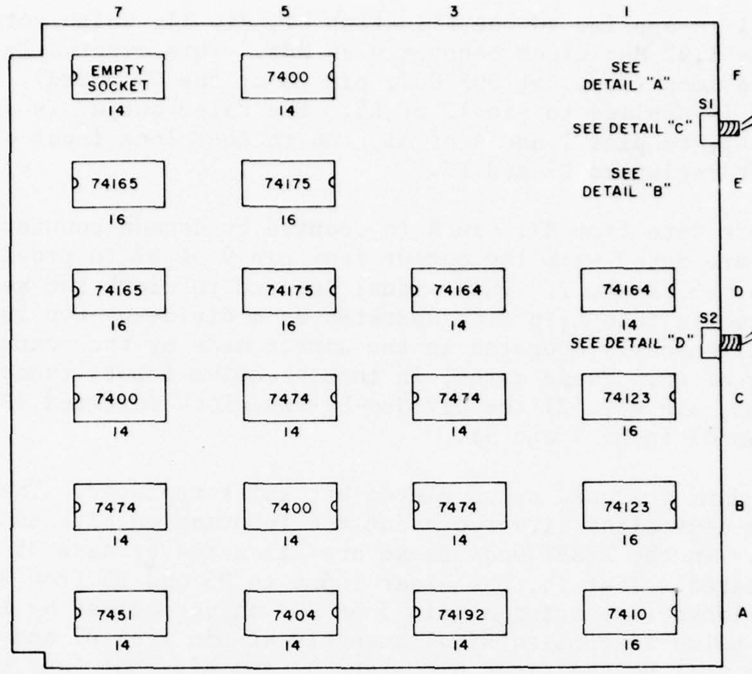
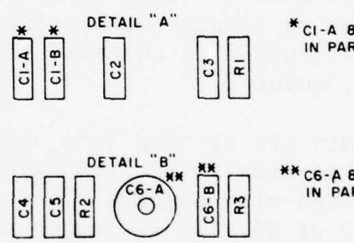


Figure 5-3. Clock Retimer Board, Logic Diagram (Sheet 2 of 2)



IDENT	LOCATION
7400	B5, C7, F5
7404	A5
7410	A1
7451	A7
7474	B3, B7, C3, C5
74123	B1, C1
74164	D1, D3
74165	D7, E7
74175	D5, E5
74192	A3



S1 - DPDT SWITCH, ON-OFF, C&K NO. 7203 SYZQ
S2 - SPDT SWITCH, C&K NO. 7101SYZQ

IDENT	LOCATION
R1, R2	20K, 1/8 W, 5% TOL.
R3	47K 1/8 W, 5% TOL.
R4	1.5 K1, 1/8 W 5% TOL.
C1-A	15,000 PF, 10% TOL., KEMET NO. CK05-BX-153K
C1-B	680 PF, 10% TOL., CENTRALAB NO. DD-681
C2	500 PF, 10% TOL., CENTRALAB NO. DD-501
C3	150 PF, 10% TOL., CENTRALAB NO. DP-151
C4	3,900 PF, 10% TOL., KEMET NO. CK05-BX-392K
C5	120 PF, 10% TOL., CENTRALAB NO. DD-121
C6-A	5-30PF VARIABLE, E.F. JOHNSON NO. 275-0430-005
C6-B	10PF, 10% TOL., CENTRALAB NO. DD-100

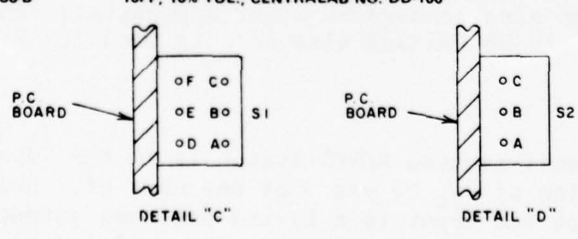


Figure 5-4. Clock Retimer Board, Parts Layout Diagram and Parts List

The clock signal is applied to the flip-flop B7, pin 11, which acts as a divide-by-two. Hence, the 1.92 MHz clock becomes 0.96 MHz. This eventually becomes the basic data rate of the loop (i.e., at BUS OUT, pin 2Q of the CR board). The true output of flip-flop B7 is applied to pin 12 of B5. The false output is applied to the input of counter A3, to pins 1 and 4 of A1, and to the clock input of the parallel-in, serial-out shift registers D7 and E7.

The divided clock rate from B7, pin 8 is counted by decade counter A3. Its outputs (pins 3 and 7) are gated with the output from pin 9 of B7 to provide waveform B5-11 shown in Figure 5-3, sheet 2. This signal is used to clock the second flip-flop of B3. Note that while this flip-flop operates as a divide-by-two in the clocked node, it is also simultaneously operated in the direct mode by the outputs from pins 6 and 12 of gates of A1. These gates, in turn, receive inputs from: (1) The inverted clock (A5, pin 6), (2) the divided-by-two clock inverted (B7, pin 8), and (3) the outputs from D7 (pins 7 and 9).

D7 and E7 together are used as an eleven bit shift register. The first bit is from B3, pin 9. The next eight bits represent the information bits and are received from D5 and E5. In the RESET mode these are all zeros because D5 and E5 are continually being cleared. That is, the clear input to D5 and E5 from B5, pin 6, occurs for every ten clocks (appearing at pin 5 of A3) as determined by the carry out from A3. A similar pulse is applied simultaneously at pin 1 of D7 and E7 to load the eight zeros, as well as the first bit, into D7 and E7. The last two bits at pins 4 and 5 of E7 are also loaded by this load pulse. However, the state of these two bits alternates as determined by flip-flop C5 operating in the clocked only mode. The clock to D7 and E7 is the same signal that clocks the counter A3. See waveforms on Figure 5-3, sheet 2.

After the inputs are strobed into D7 and E7 by D7-1 of Figure 5-3, sheet 2, they are clocked out from pins 9 and 7 of D7 by signal B7-8 of Figure 5-3, sheet 2. These outputs are gated with signals B7-8 and B7-11 (after inversion) and applied to inputs 10 and 13 of B3. These inputs together with the clocked input at pin 12 of B3 result in the output of B3-8 on Figure 5-3, sheet 2. This signal represents the frame format and consists of the address field identifier (A), the eight information bits of the address field (all zeros), the data field identifier (D), and the eight information bits of the data field (all zeros). Note that zeros are highs in signal B3-8. This signal, or frame format, is delivered to the first LIU board in the loop. It is described in the LIU description of paragraph 5.2.8.

It should be noted that the output from pin 8 of B3 is connected directly to pin 2Q of the CR Board, via strapping on the back of F7, and chip F7 is removed. Hence, a TTL output exists at pin 2Q. An EIA output could be provided at this point by removing the strapping, installing an MC1488L chip in location F7 and connecting the necessary negative and positive voltages at pins 1 and 14 of F7. EIA receivers and transmitters would then also be used at other appropriate locations such as the inputs and outputs of the LIU Boards and also at chip location F5 of the CR Board.

5.2.2.2 Normal Mode

In the normal mode, the panel-mounted RESET switch is in the "down" (open) position resulting in the application of V_{cc} to pin 3 of one shot C1. Hence, the one shot responds to rising edges of its input (pin 2) and produces output pulses of approximately 150 nanoseconds. These pulses cause flip-flops B3 and C5 to operate in the

direct mode as well as the clocked mode; and, also clock the flip-flops of D5 and E5.

The Loop signal, from the preceding LIU Board, is received at pin 2E of the CR Board. The signal is received by the Bus receiver F5 and applied to A5, pin 1; A7, pin 3; and B7, pin 2. This logic (A5, A7 and B7) provides a standardized noise free bus input to the CR board. The signal at pin 6 of A7 is a narrow pulse corresponding to each transition of the loop signal and strobes the Loop signal into the flip-flop B7. The Loop signal, delayed, then appears at the output (pin 5) of B7. This logic is the same as that contained in the input section of the LIU Board. Specific waveforms and their relationships are shown in Figure 5-27 of the LIU Board description (paragraph 5.2.8).

With the ODD/EVEN switch in the EVEN position, the output from pin 5 of B7 is connected directly to the input (pin 12) of C3. However, in the ODD position a nine bit delay (provided by flip-flop C3 and shift register D1), which is equivalent to the delay within an LIU Board, is added to the signal before it is applied to pin 12 of C3. Referring to Figure 5-27, sheet 1, it is seen that each transition on the loop results in a pulse at pin 6 of A7 (refer to CBID waveform). These pulses are applied to the inputs (pins 10 and 2) of the one shots of B1. The pulse widths of these one shots are determined by the position of switch S1 and are indicated by note 1 on Figure 5-3, sheet 1. The BUS IN signal on Figure 5-27, sheet 1, consists of a C-field identifier (two clocks wide), eight data pulses (each one clock wide), a D-field identifier (two clocks wide) and eight more data pulses. The first half of each data pulse corresponds to clock and the second half corresponds to information. The clock and the data positions may both be in the same state or they may be in opposite states. In either case, the data position is strobed by a separate strobe signal that occurs at the three-quarter point of the referenced clock signal (1 MHz) in Figure 5-27, sheet 1. This strobe appears at pin 12 of B1 and corresponds to T3 in Figure 5-27, sheet 2. Hence the information contained in the signal received from the loop is strobed into flip-flop C3 and shifted through D1 and C3 into D3.

After each set of eight information bits (corresponding to a C-field or a D-field) are strobed into D3, they are transferred to the flip-flops of D5 and E5. The clear and clock signals associated with D5 and E5 are derived by the one shots of B1 and C1. The output of B5 at pin 3 (pulses associated with each transition of the received loop signal) is used to trigger B1 at pin 2. Since the period of B1's pin 4 output is 1.25 times the referenced clock, the pin 4 output is retriggered (held low) by each input pulse (see T3 of Figure 5-27, sheet 2) that occurs at the referenced clock rate. Hence, a rising edge occurs at pin 4 only when the input pulses are separated by the period of the C or D identifier. That is, the output at pin 4 corresponds to the MCC signal on Figure 5-27, sheet 2. (Note that since B1 is being retriggered, its output pulse duration must be measured with respect to the last rising edge preceding a C or D identifier.)

The output from pin 4 of B1 triggers the one shot C1 which, in turn, generates output pulses of apprximately 150 nanoseconds duration. The output at pin 13 of C1 is applied to pins 1 and 5 of C7 and to the clock inputs of flip-flops D5 and E5. Hence, when the output pulse occurs at pin 13 of C1, the eight information bits of the C field or D field are present in D3 and are strobed into D5 and E5. Also, at this time the succeeding C-field or D-field identifier is present at pins 8 and 9 of flip-flop C3 and is strobed by the pulse from C1, pin 13, into flip-flop C5. When the load pulse is applied to pin 1 of D7 and E7, these registers are loaded

with the bits from D5 and E5, the C-field or D-field identifier from C5, and the last output bit from B3. After loading D7 and E7, operation proceeds as described in the latter part of previous section describing the reset mode.

While the normal frame sequence is being received at input 2E of the CR Board, a pulse is output from pin 4 of C1 presetting B3 for each field. Thus the output at pin 6 of B3 remains low and no clock is applied to pin 11 of C5. However, if B3 is not preset, an output is generated at pin 6 of B5 thereby clocking flip-flop C5 and generating alternating C and D field identifiers for application to pins 4 and 5 of E7. This operation is as described under the previous section dealing with the reset mode.

5.2.3 B7* MICROPROCESSOR

The B7* microprocessor consists of two PC Boards identified as the MD1 Board and the MD2 Board. Each board consists of TTL logic, and together they perform data processing in 8-bit bytes; i.e., each instruction operates on eight bits of data. The two boards must be mounted in adjacent slots of the backplane and interconnected at their front edges (front plane) via a front-plane connector. (See Figures 5-5 thru 5-15.)

5.2.3.1 ESM Configurations

The B7* microprocessor is used in the ESM in two separate configurations: (1) Node Control Unit (NCU), and (2) Control and Interface Equipment (CIE). In the NCU configuration the MD1 Board has the following options implemented:

a. PROM is used for microprogram memory. The PROM consists of 256 words (12 bits each), and is implemented in the form of three chips (each 256 X 4) in chip locations E5, E7, and E9 on the MD1 Board. See Figure 5-12, sheet 2, and Figure 5-13.

b. The Microprogram Count Register (MPCR) (C5, C7, C9) is configured for eight bits. MPCR chips in locations C3 and C5 are removed. See Figure 5-12, sheet 4, and Figure 5-13.

c. The Alternate Microprogram Count Register (AMPCR) (B3, B5, B7, B9) is configured for eight bits. AMPCR chips in locations B3 and B5 are removed. See Figure 5-12, sheet 4, and Figure 5-13.

d. The selector chips (A5, A7, A9) associated with the MPCR and the AMPCR are configured for eight bits. Selector chips in locations A3 and A5 are removed. See Figure 5-12, sheet 4, and Figure 5-13.

e. In connection with item c. above, a jumper is installed from pin 3 of B3 to pin 12 of B5. See Figure 5-12, sheet 4.

f. The SKIP 2 is disabled by a jumper from pin 10 of E1 to ground, and the connection removed between pin 10 of E1 and pin 1 of E1. See Figure 5-12, sheet 5.

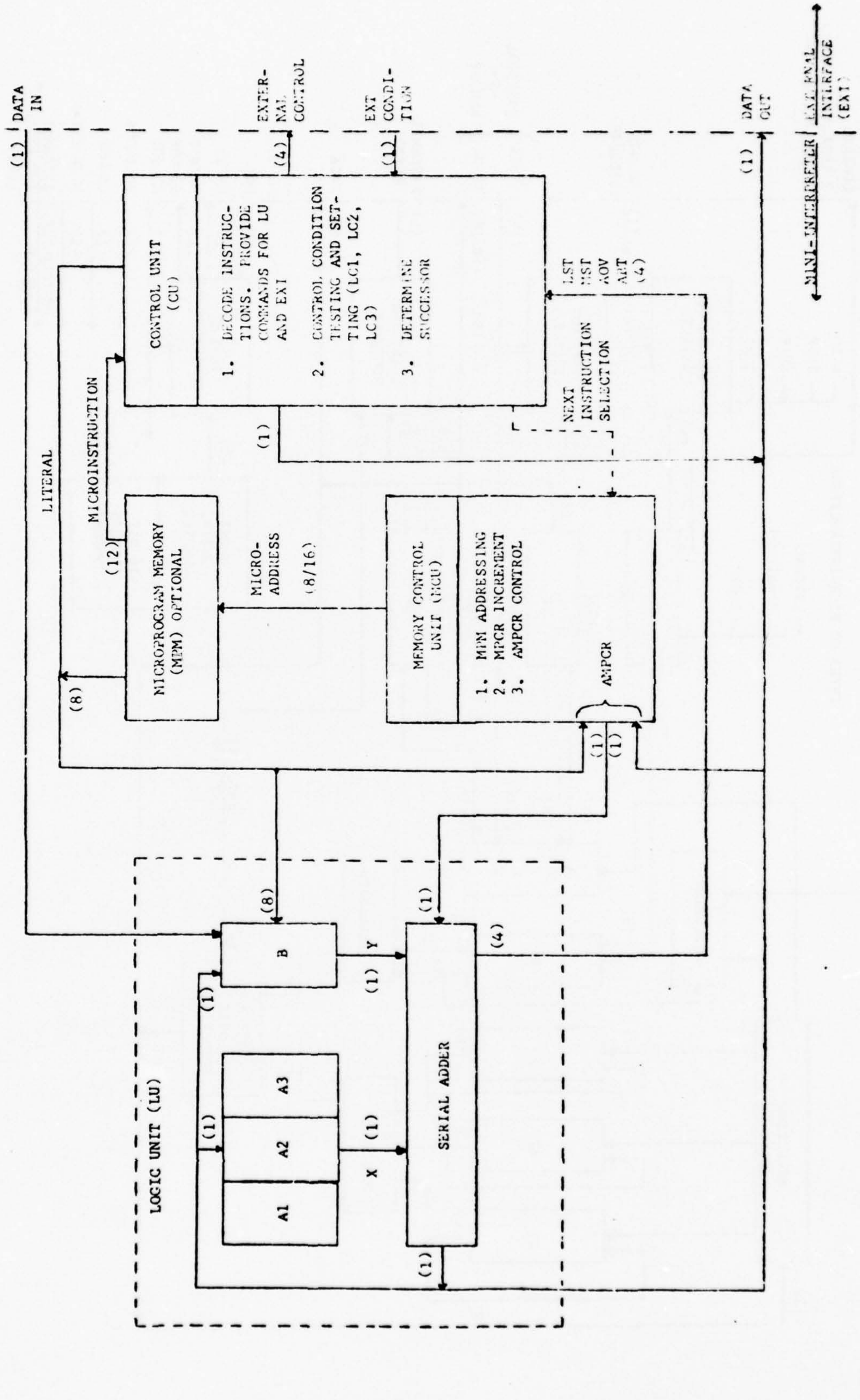


Figure 5-5. B7* General Block Diagram

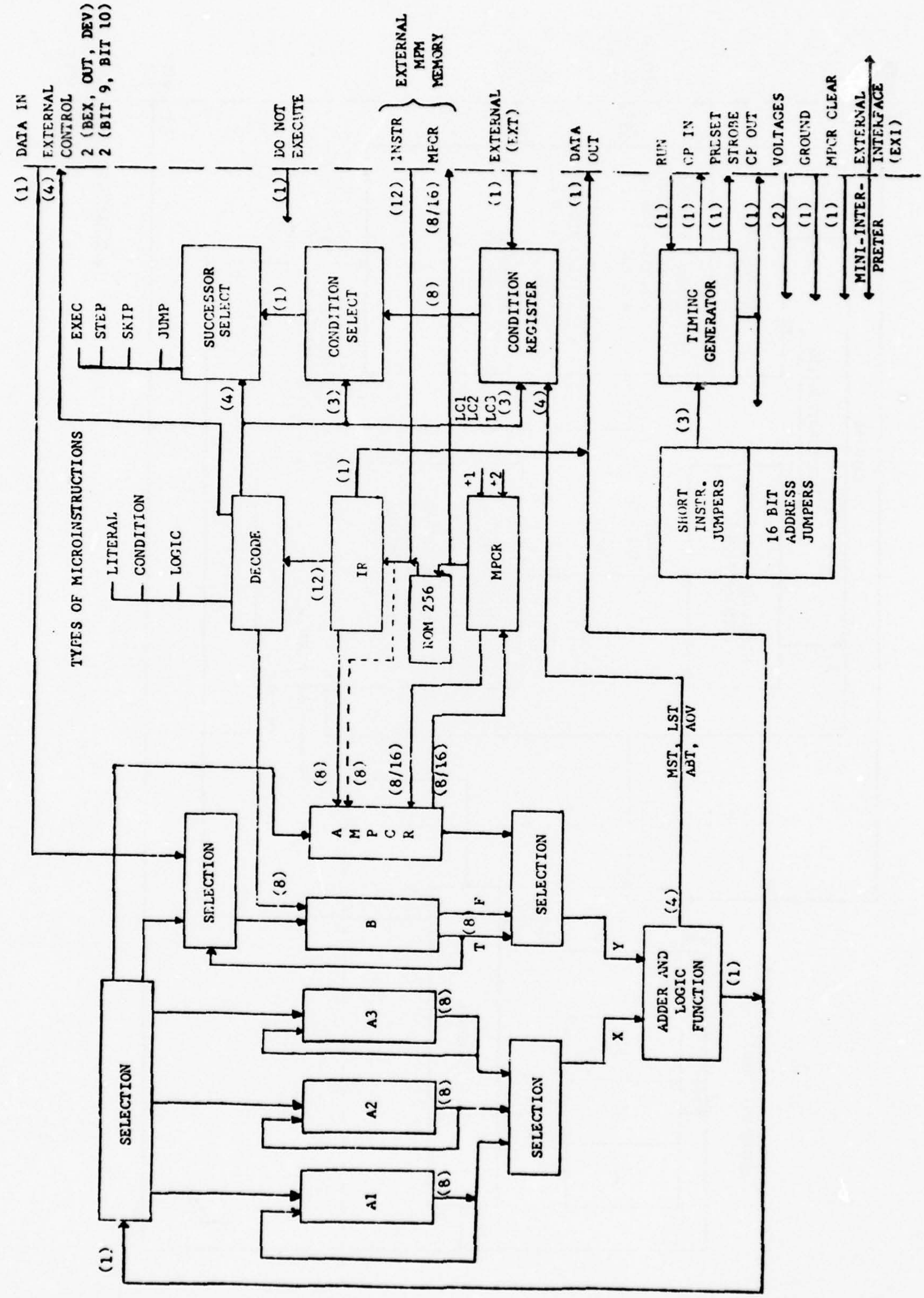


Figure 5-6. General Purpose Block Diagram

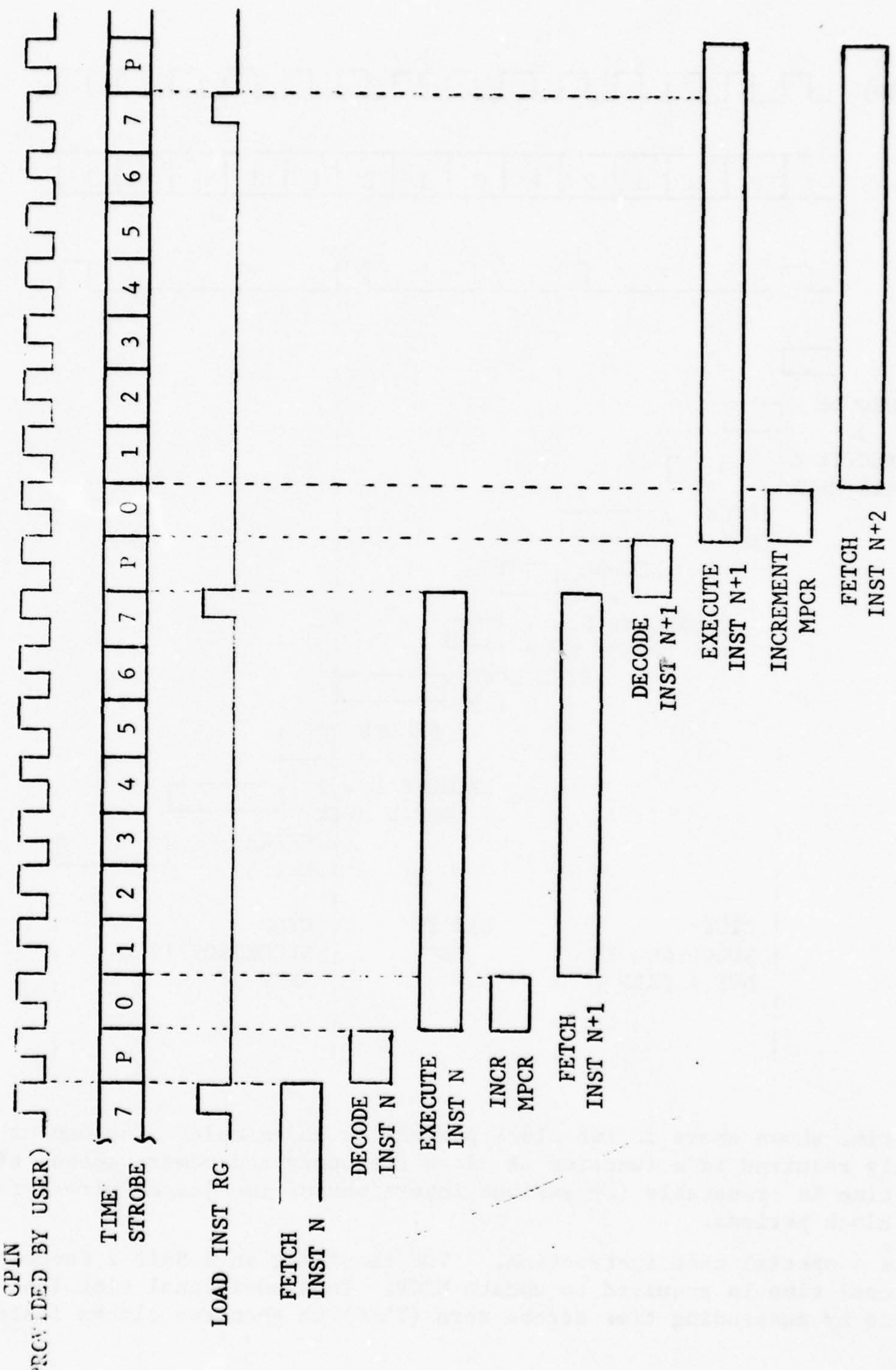
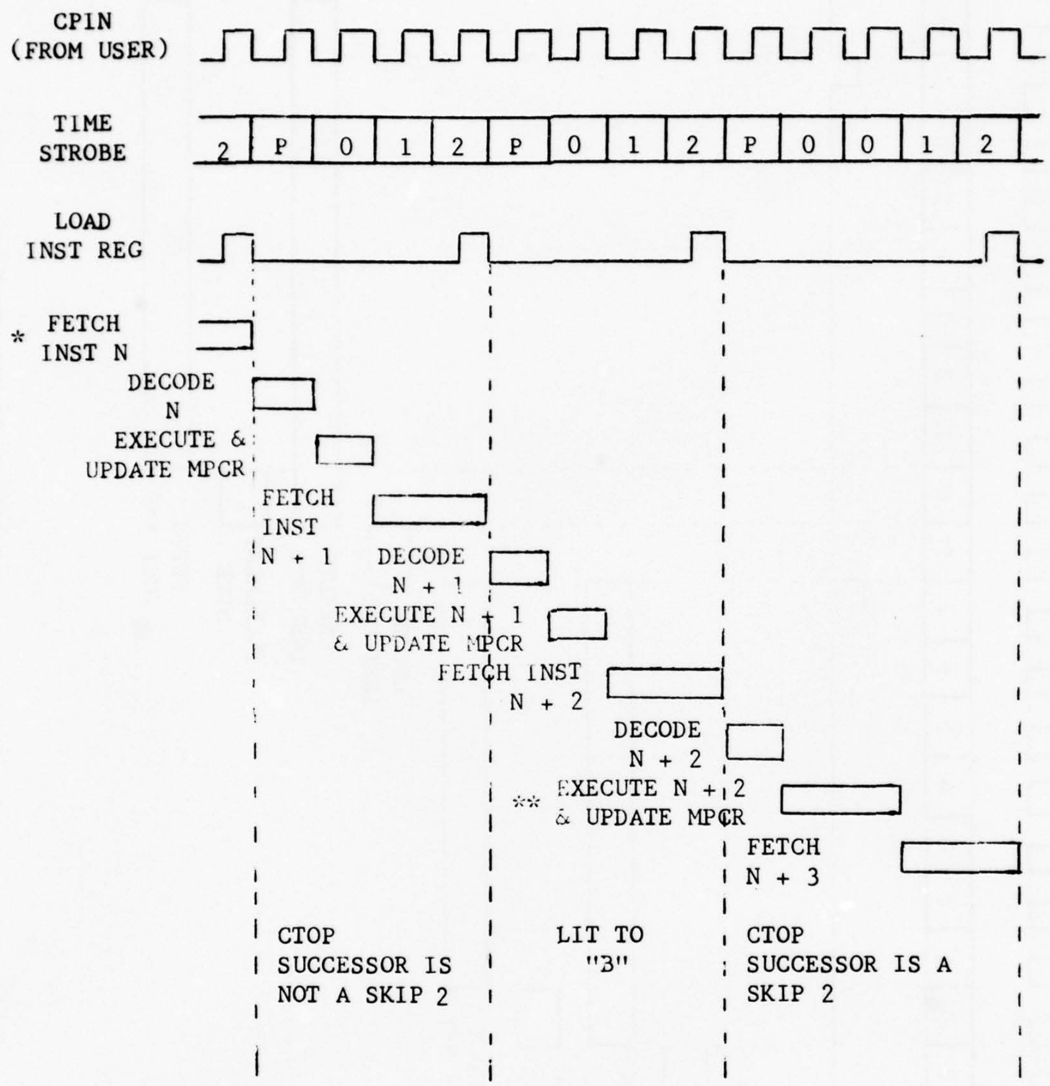


Figure 5-7. Timing Diagram of a Logic Unit or LITERAL-TO-DEVICE Instruction



* Fetch time shown above is two clock periods as an example. The number of clocks actually required is a function of clock frequency and memory access time. The fetch time is presetable (by various insertions of two jumper wires) from one to eight clock periods.

** This is a special case instruction. CTOP resulting in a SKIP 2 Successor where additional time is required to update MPCR. This additional time (one clock) is acquired by suspending time strobe zero (TSB0) to span two clocks instead of one.

Figure 5-8. Timing Analysis of Instructions Other than LITERAL-TO-DEVICE or LUOPS

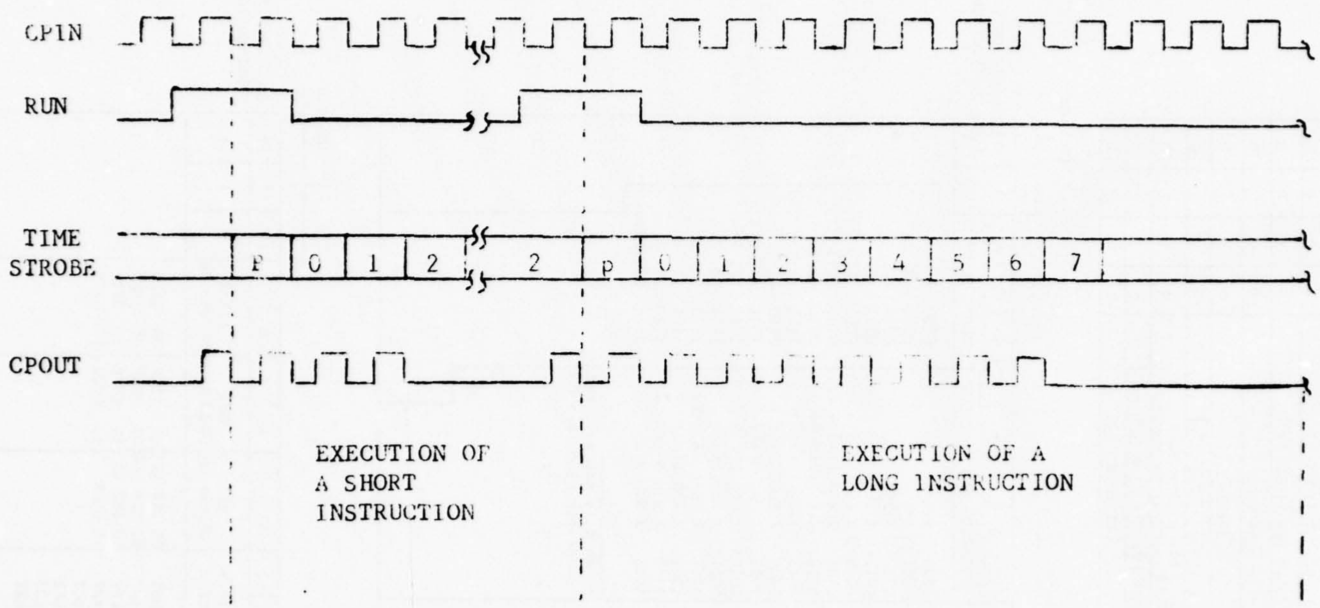


Figure 5-9. Timing Analysis of Single Instruction Mode

LITERAL INSTRUCTIONS (OP CODE: bits 9–12)

1–8	9	10	11	12
LIT. TO DEV (PORT 0)	0	0	0	0
LIT. TO DEV (PORT 1)	0	1	0	0
LIT. TO DEV (PORT 2)	1	0	0	0
LIT. TO DEV (PORT 3)	1	1	0	0
SPARE	0	0	1	0
SPARE	1	0	1	0
CALL (MPCR+1 → AMPCR, LIT & IR → MPCR)	0	1	1	0
GOTO (LIT & IR → MPCR, AMPCR IS UNCHANGED)	1	1	1	0
LIT. TO IR (MS ADR BYTE FOR 16 BIT GOTO OR CALL)	0	0	1	1
LIT TO B	1	C	1	1

LOGIC UNIT INSTRUCTION (OP CODE: bits 11–12)

1–2: X SELECT	3–7: OPERATION AND Y SELECT	7–10: DEST. SELECT	11	12
00 0	0000 X+B+1	0000 B	0	1
01 A1	0001 X+B	0001 A1		
10 A2	0010* X+Z+1	0010 A2		
11 A3	0011* X+Z	0011 A3		
	0100 X EQV B(XB v $\overline{X}\overline{B}$)	0100 OUT0		
	0101 X XOR B($X\overline{B}$ v $\overline{X}B$)	0101 OUT1		
	0110 X-B ($X+\overline{B}+1$)	0110 OUT2		
	0111 X-B-1 ($X+\overline{B}$)	0111 AMPCR, OUT3		
	1000 X NOR B($\overline{X \text{ v } B}$)	1000 B, BEX		
	1001 X NAN B($\overline{XB}$)	1001 A1, BEX		
	1010* X NOR Z($\overline{X \text{ v } Z}$)	1010 A2, BEX		
	1011* X NAN Z($\overline{XZ}$)	1011 A3, BEX		
	1100 X OR B (X v B)	1100 B S		
	1101 X AND B(XB)	1101 A1 S		
	1110 X RIM B (X v $\overline{B}$)	1110 A2 S		
	1111 X NIM B($\overline{XB}$)	1111 A3, AMPCR		

*When Z is not selected as destination, Z = 0.

CONDITION TEST INSTRUCTION (OP CODE: bits 10–12)

1–3: CONDITION SELECT	4–5: SET OPERATION	6–7: TRUE SUCCESSOR	8–9: FALSE SUCCESSOR	10	11	12
000 MST	00 SET LC1	00 STEP	00 STEP	1	1	1
001 AOV	01 SET LC2	01 JUMP	01 JUMP			
010 LST	10 SET LC3	10 SKIP	10 SKIP			
011 ABT	11 NONE	11 EXEC	11 EXEC			
100 LC1						
101 LC2						
110 LC3						
111 EXT						

Figure 5-10. B7* Instruction Set

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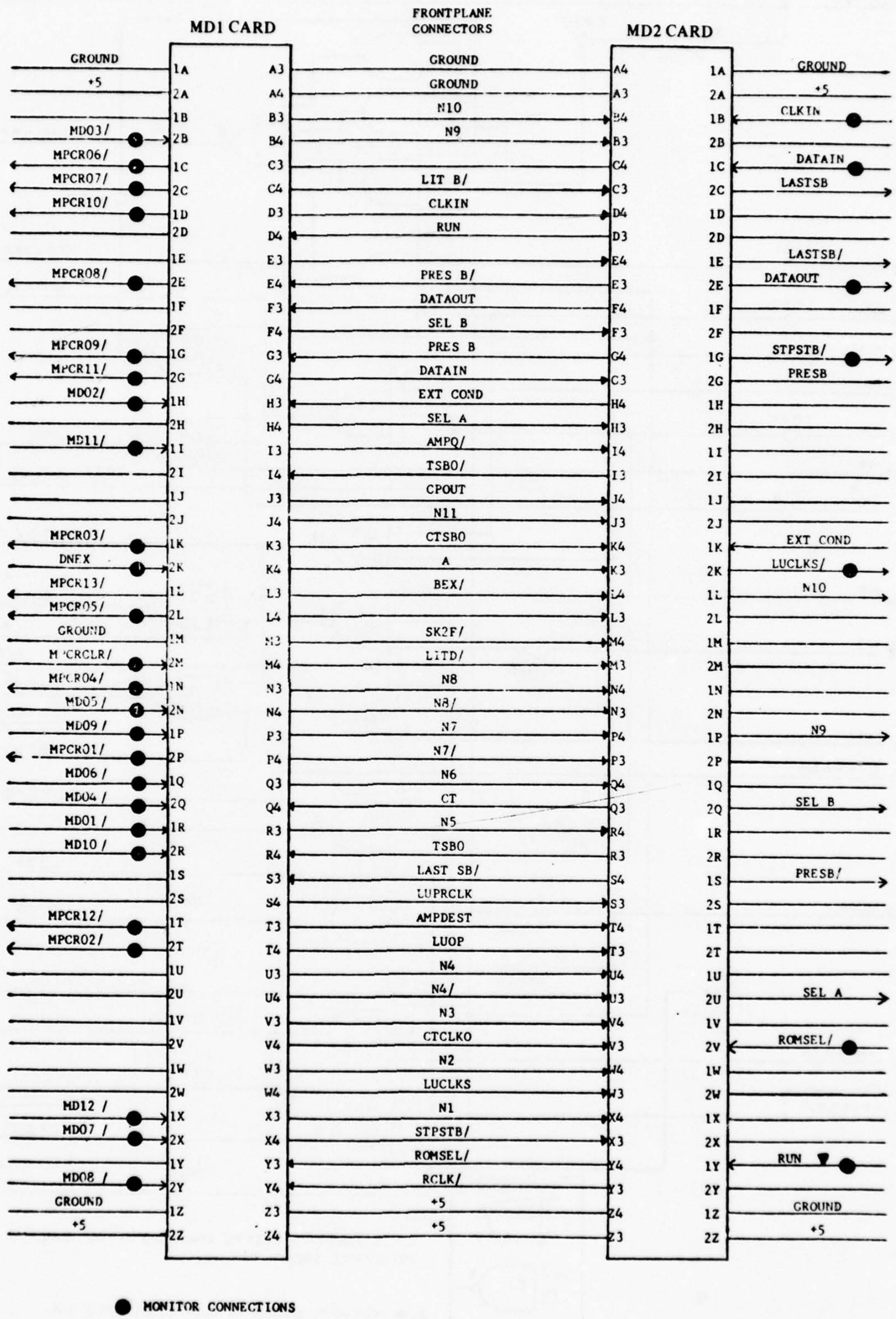

Figure 5-11. B7* Interface Wiring

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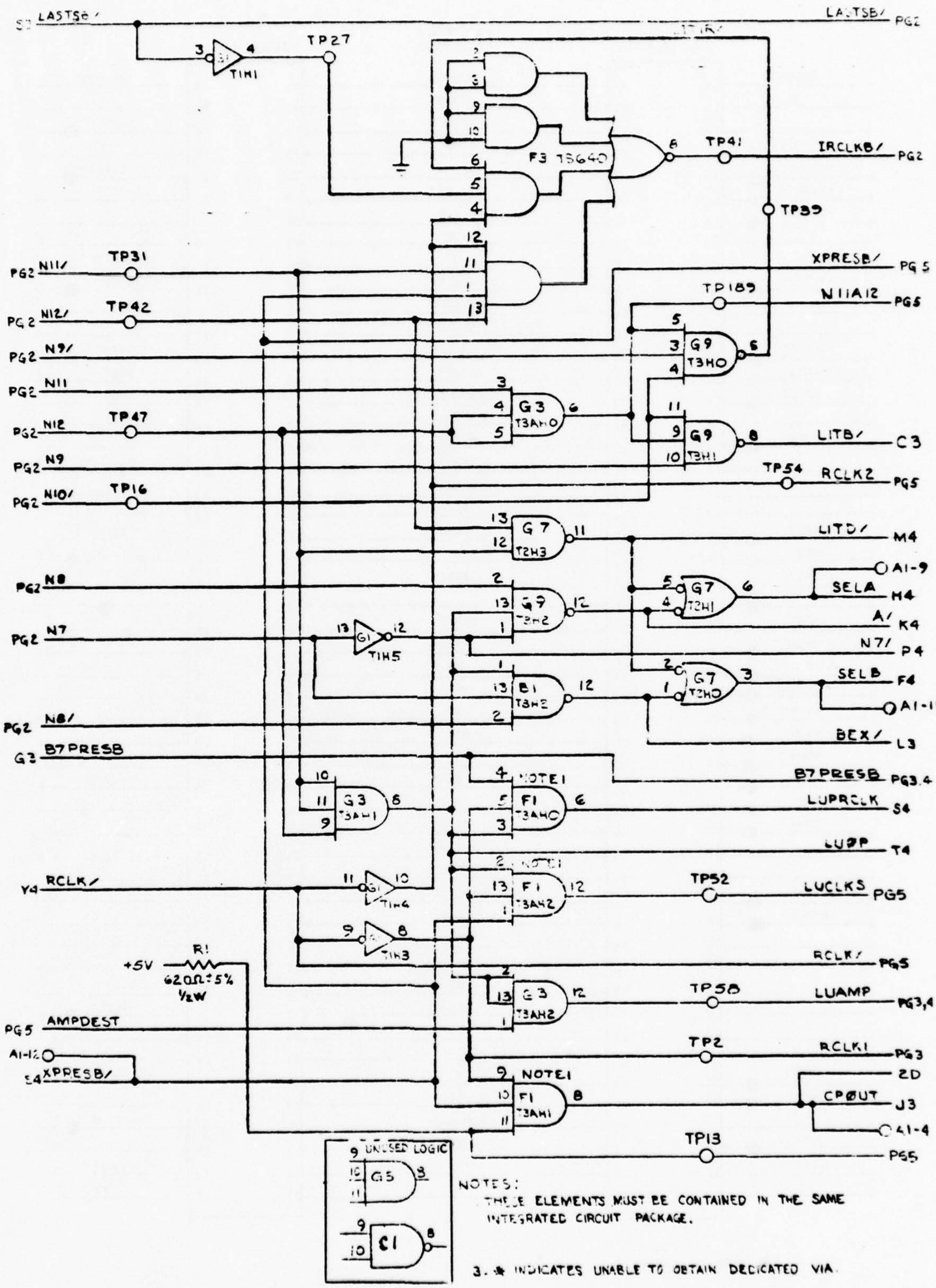

Figure 5-12. NCU and CIE MD1 Board Logic (Sheet 1 of 5)

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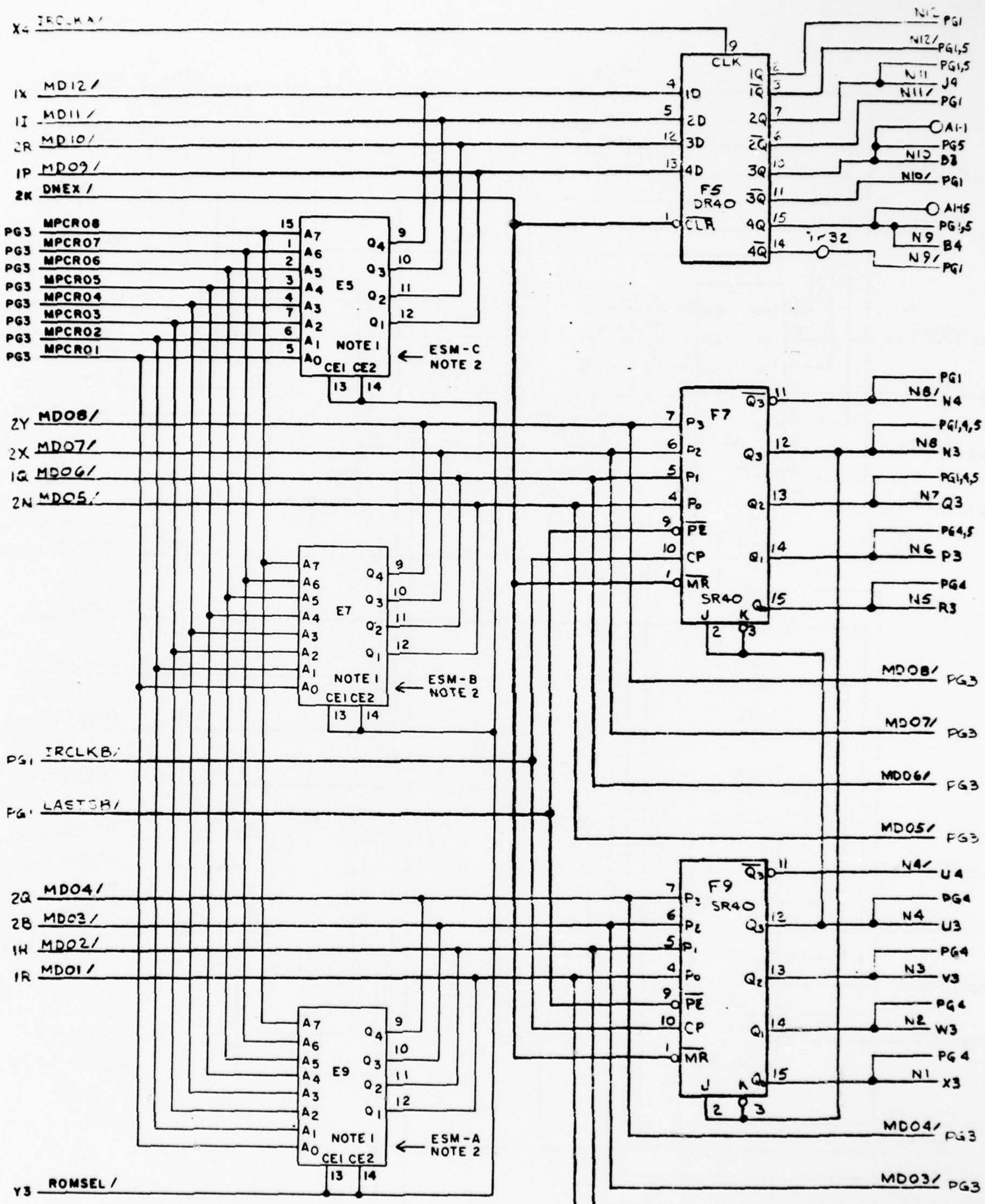

NOTES:
1. SOCKET & CHIP ARE INSTALLED ONLY ON NCU MD1 BOARD.
2. FOR COMPLETE CHIP PART NUMBER REFER TO BOARD LAYOUT (SHEET 6)

Figure 5-12. NCU and CIE MD1 Board Logic (Sheet 2 of 5)

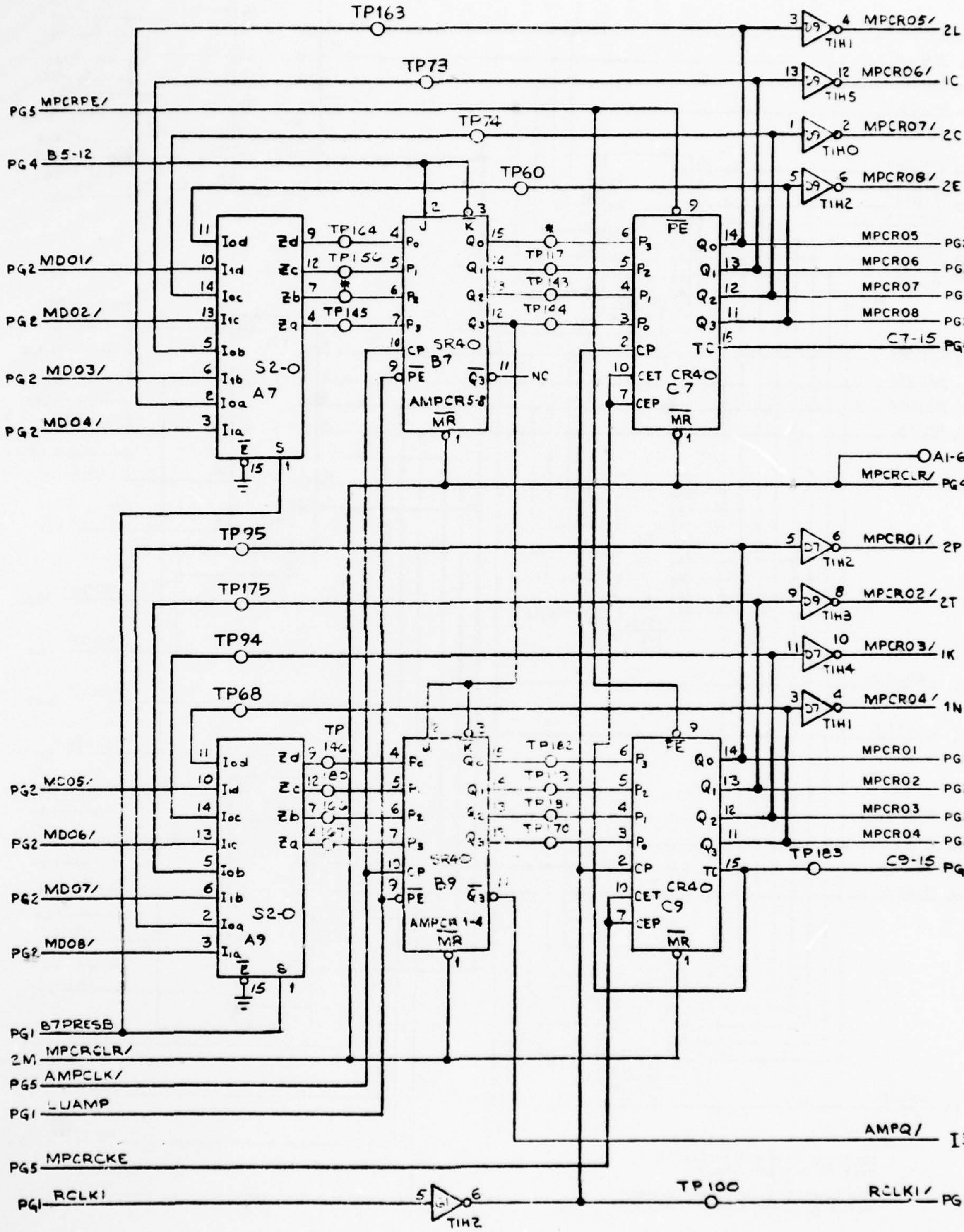

Figure 5-12. NCU and CIE MD1 Board Logic (Sheet 3 of 5)

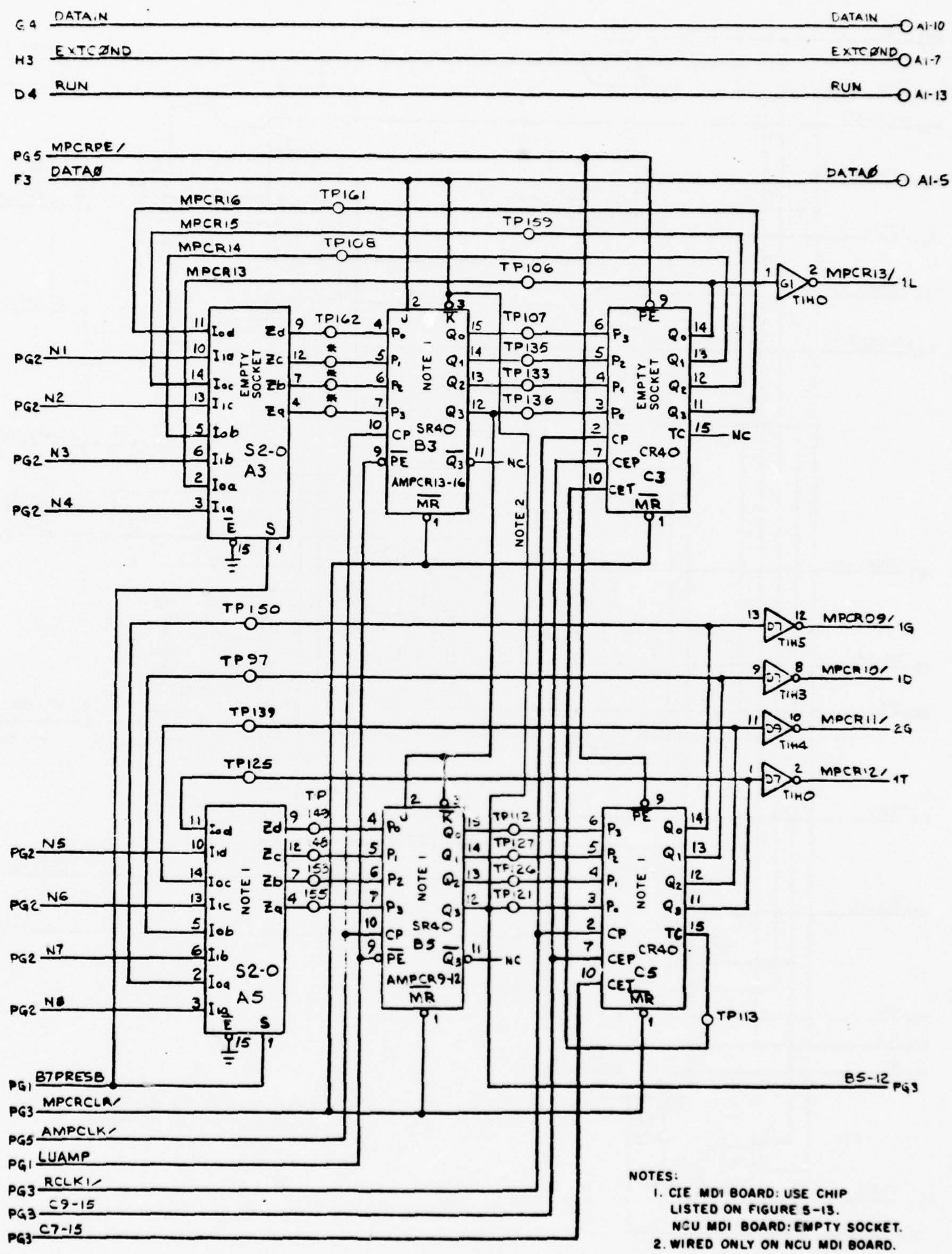

Figure 5-12. NCU and CIE MD1 Board Logic (Sheet 4 of 5)

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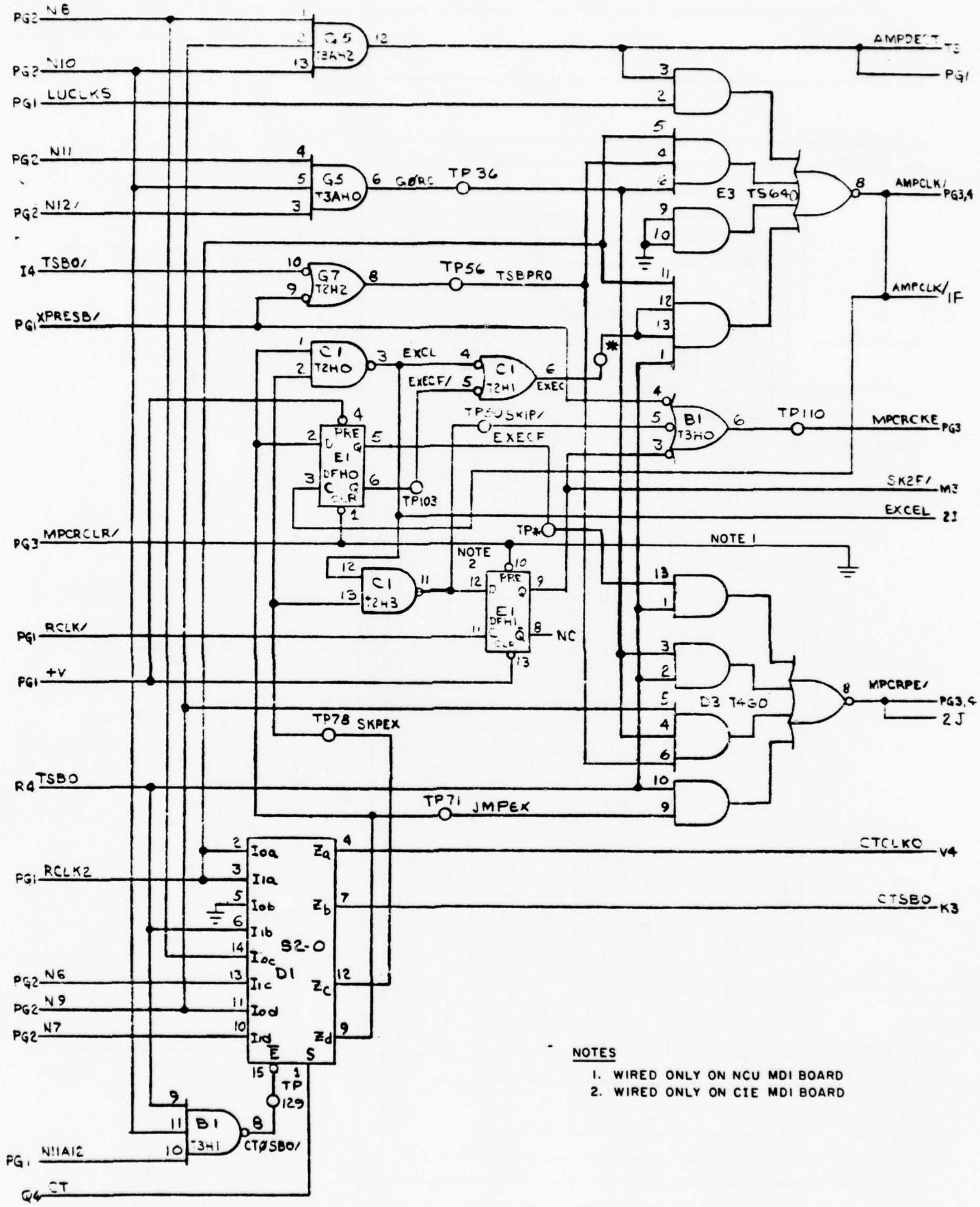

Figure 5-12. NCU and CIE MD1 Board Logic (Sheet 5 of 5)

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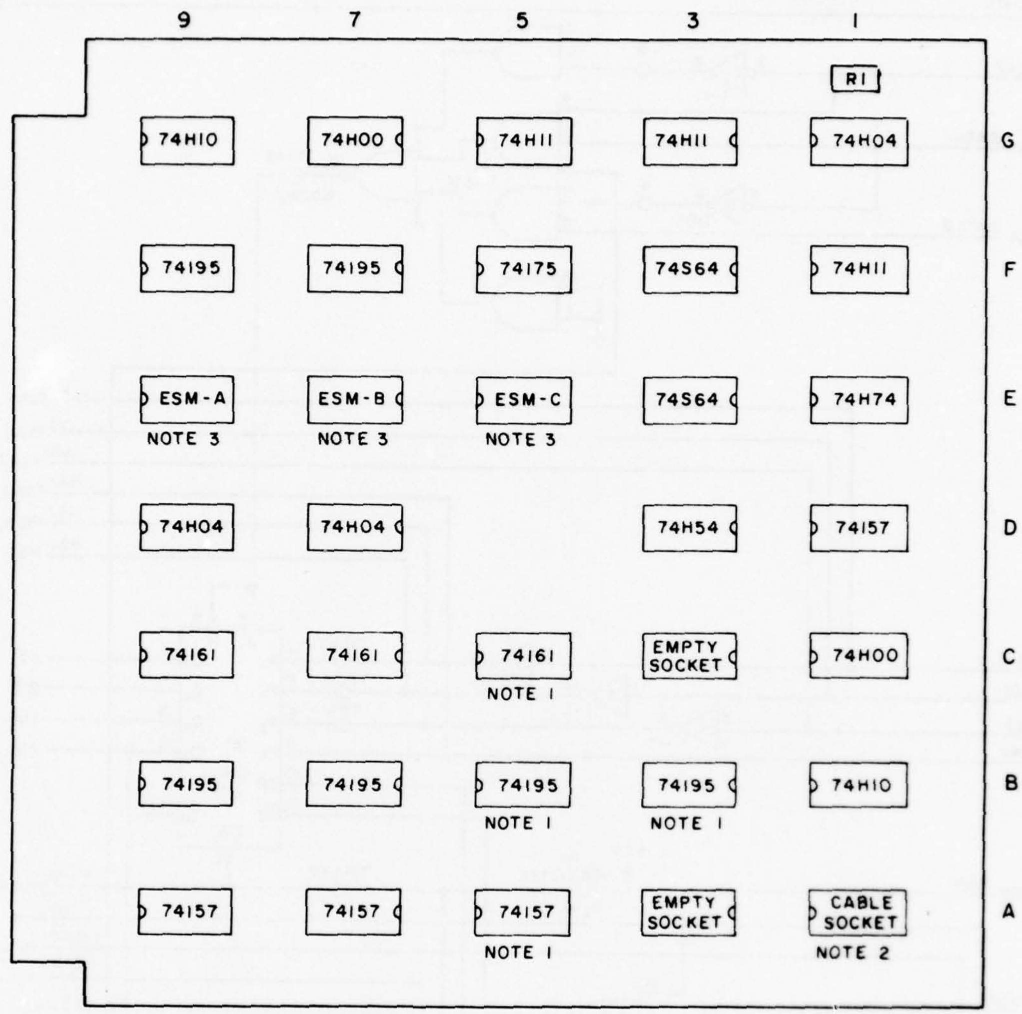


IDENT	LOCATION
74H00	C1, G7
74H04	D7, D9, G1
74H10	B1, G9
74H11	F1, G3, G5
74H54	D3
74S64	E3, F3
74H74	E1
74157	A5 (CIE ONLY), A7, A9, D1
74161	C5 (CIE ONLY), C7, C9
74175	F5
74195	B3 (CIE ONLY), B5 (CIE ONLY) B7, B9, F7, F9
HARRIS	# HMI-7611-5-ESM-A Board Location E9
HARRIS	# HMI-7611-5-ESM-B Board Location E7
HARRIS	# HMI-7611-5-ESM-C Board Location E5
R1	620 OHM, 1/2 W, 5% TOL.

NOTES

ALL PARTS APPLY TO BOTH NCU AND CIE BOARDS UNLESS OTHERWISE SPECIFIED BY NOTES.

1. CHIP SPECIFIED APPLIES ONLY TO CIE, AN EMPTY SOCKET APPLIES TO NCU.
2. CABLE SOCKET APPLIES ONLY TO NCU, AN EMPTY SOCKET APPLIES TO CIE.
3. PROM CHIP SPECIFIED IN PARTS LIST APPLIES ONLY TO NCU, THERE IS NO SOCKET FOR CIE. THE ESM-A, B, C PORTION OF THE PART NUMBER SPECIFIES THE MEMORY PROGRAM BURNED INTO THE CHIP.

Figure 5-13. NCU and CIE MD1 Board, Parts Layout Diagram and Parts List

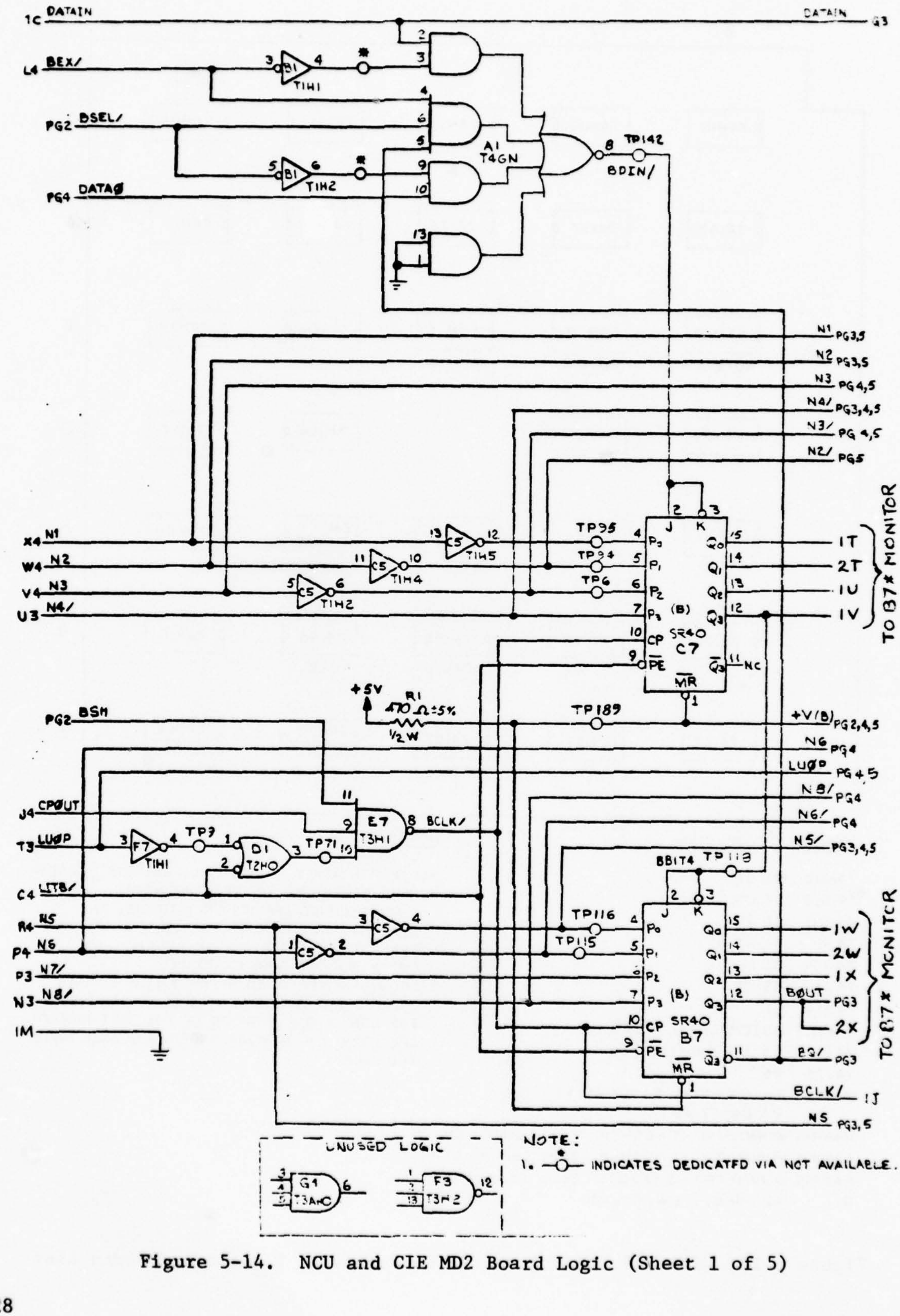


Figure 5-14. NCU and CIE MD2 Board Logic (Sheet 1 of 5)

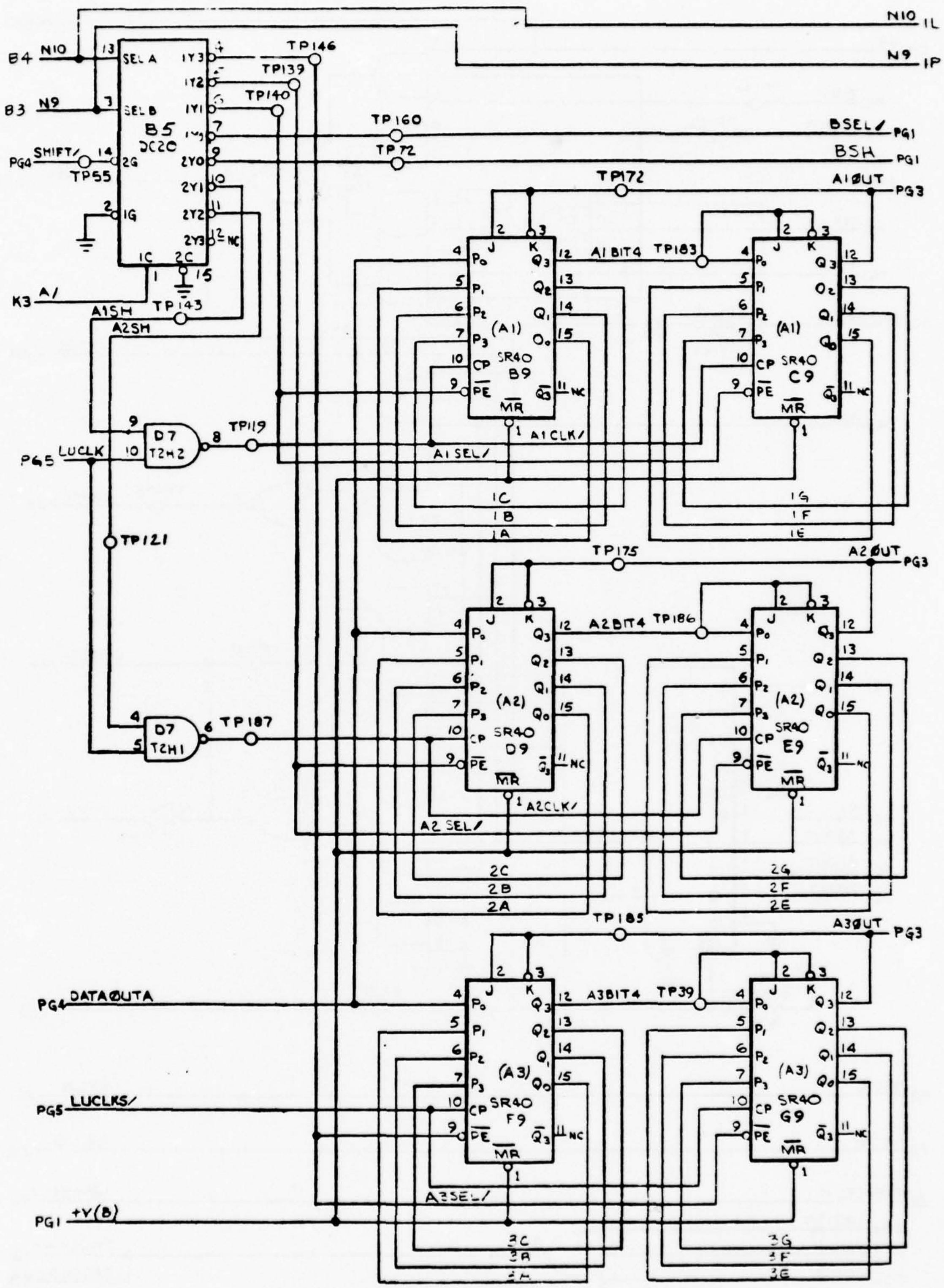


Figure 5-14. NCU and CIE MD2 Board Logic (Sheet 2 of 5)

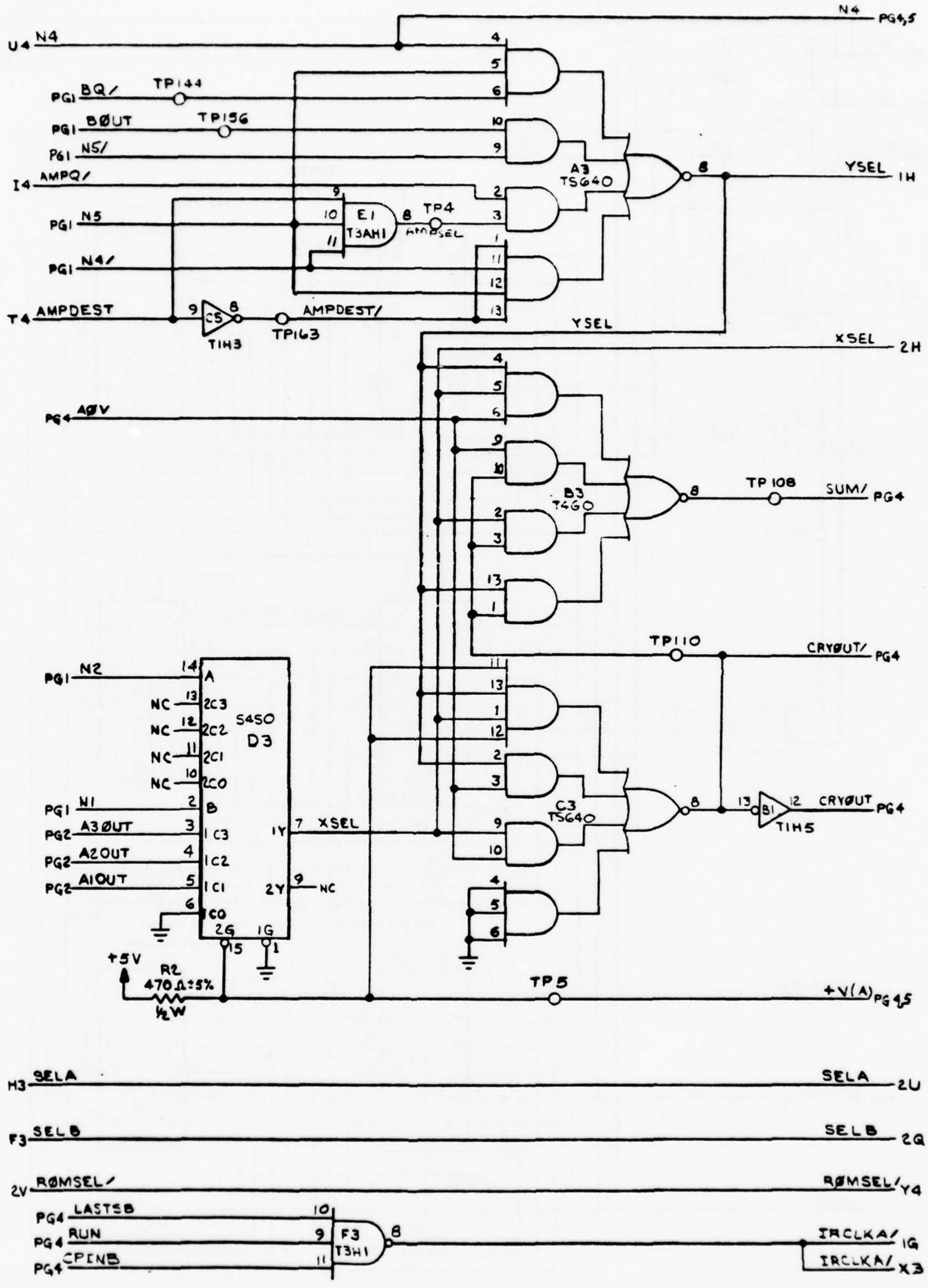


Figure 5-14. NCU and CIE MD2 Board Logic (Sheet 3 of 5)

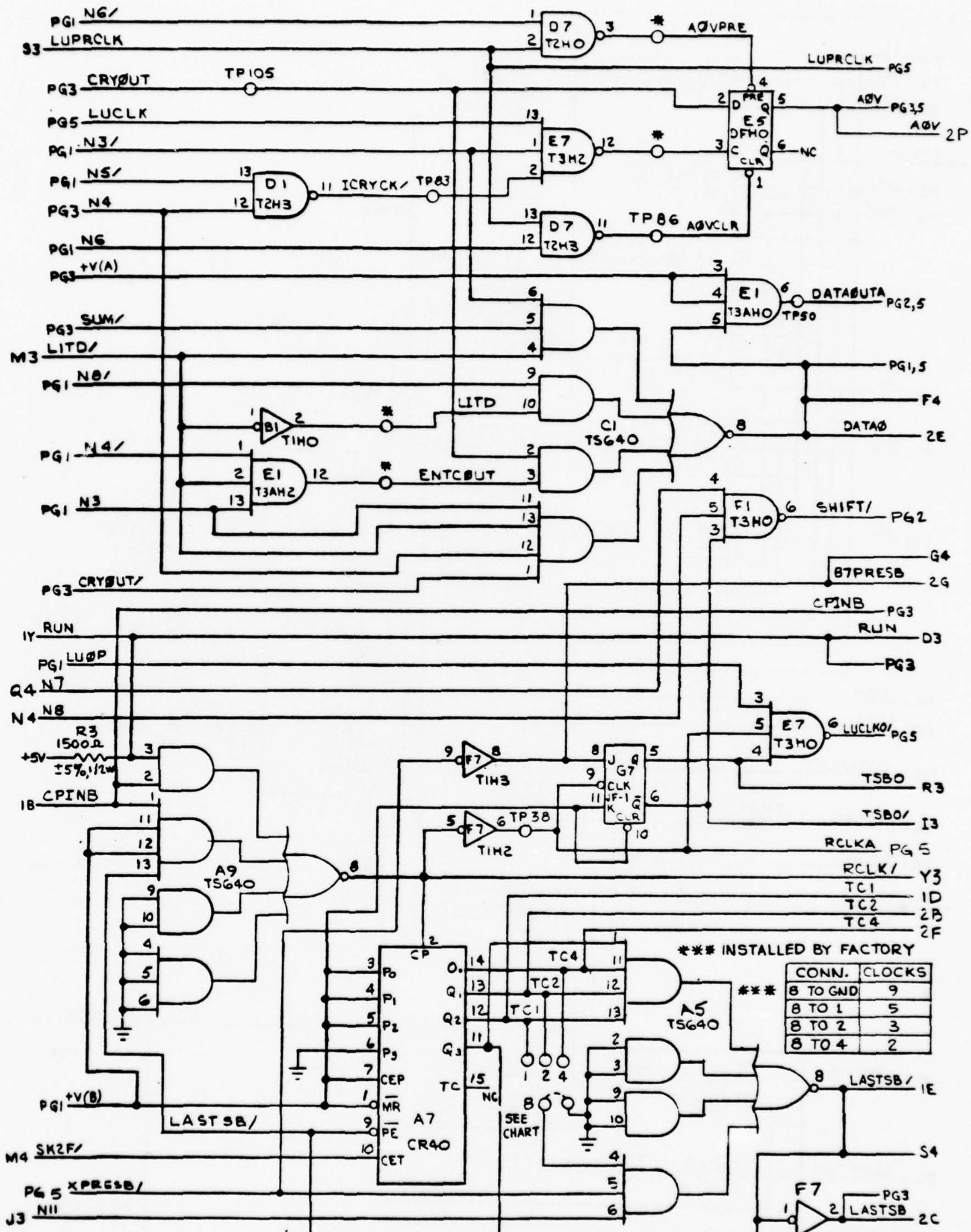


Figure 5-14. NCU and CIE MD2 Board Logic (Sheet 4 of 5)

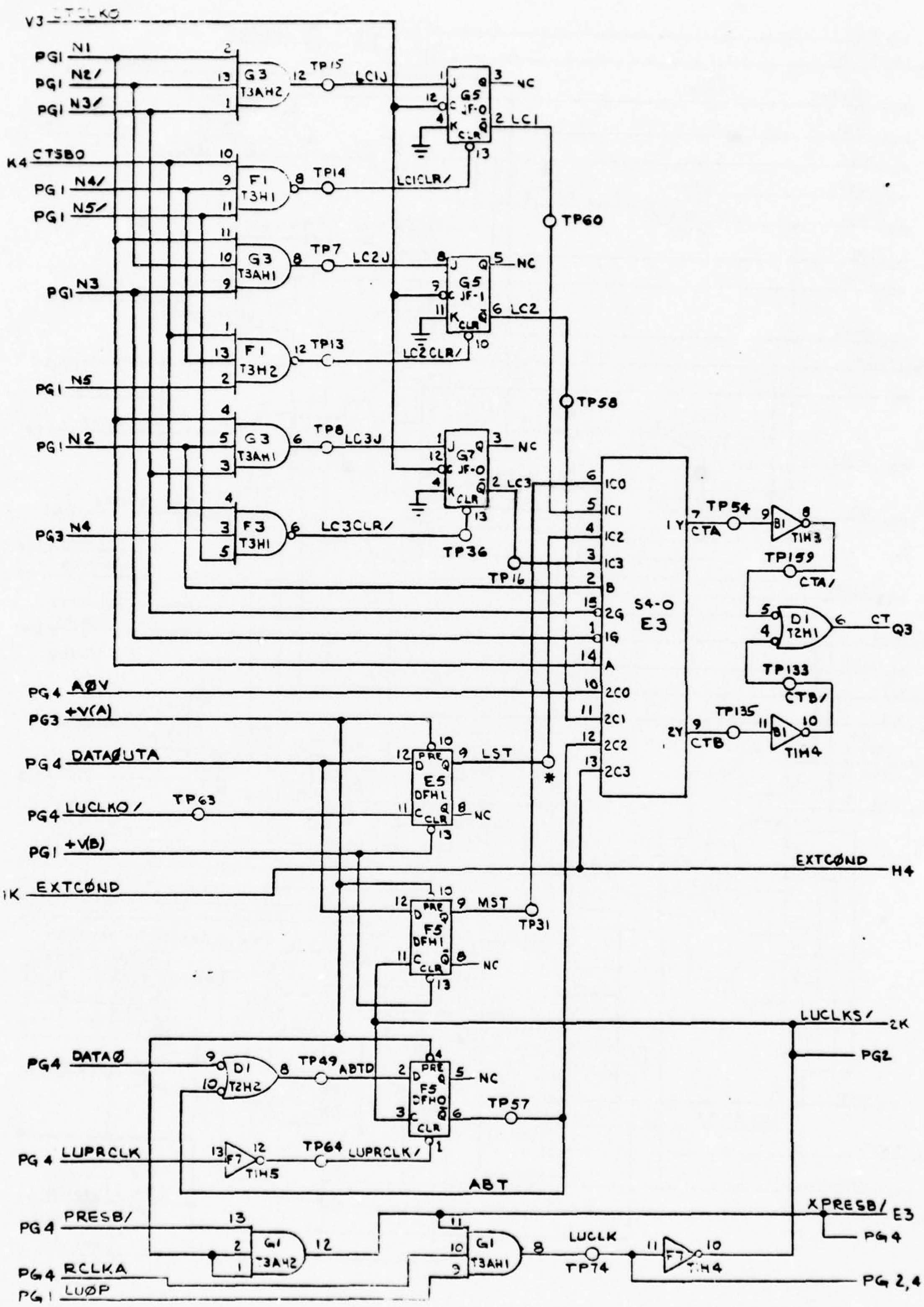
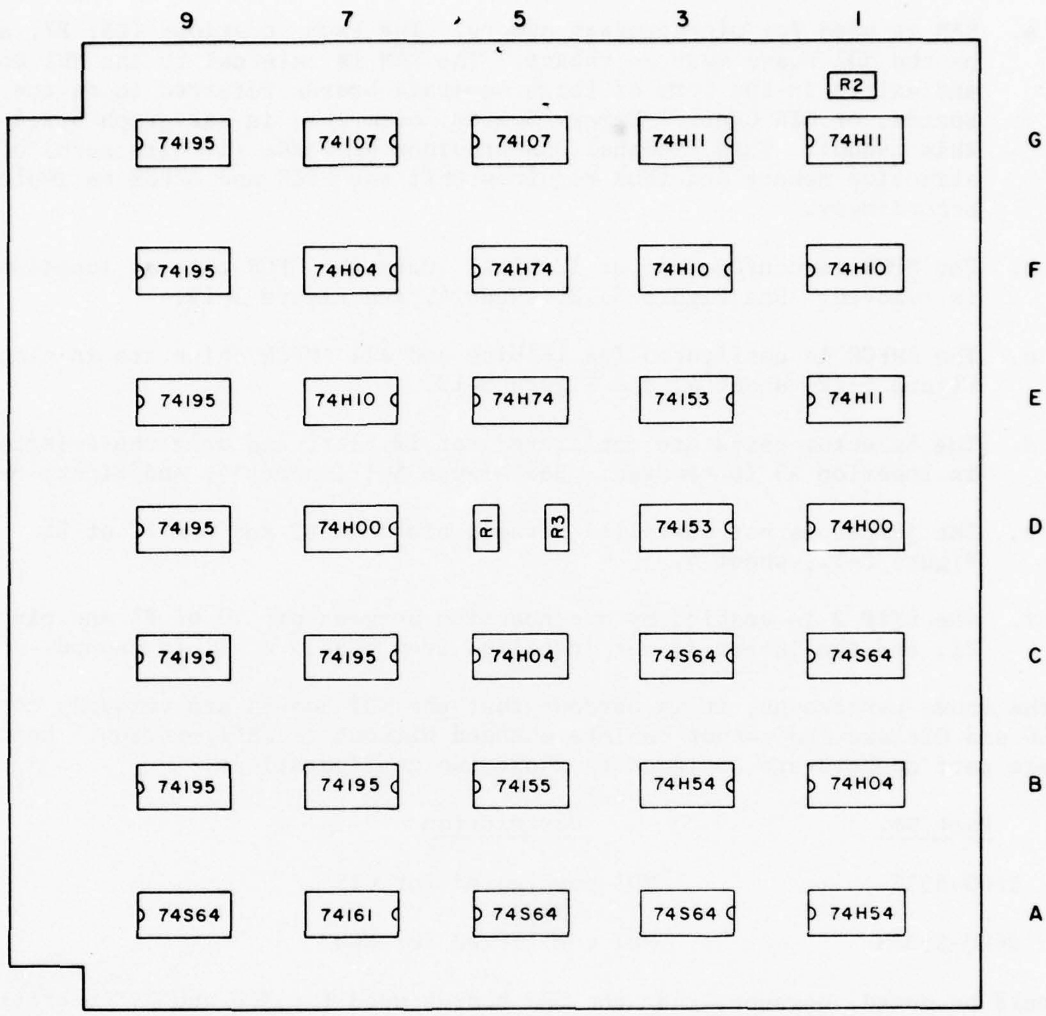


Figure 5-14. NCU and CIE MD2 Board Logic (Sheet 5 of 5)



IDENT	LOCATION
74H00	D1, D7
74H04	B1, C5, F7
74H10	E7, F1, F3
74H11	E1, G1, G3
74H54	A1, B3
74S64	A3, A5, A9, C1, C3
74H74	E5, F5
74107	G5, G7
74153	D3, E3
74155	B5
74161	A7
74195	B7, B9, C7, C9, D9, E9, F9, G9

IDENT	VALUE
R1, R2	470 OHM, 1/2 W, 5% TOL
R3	1500 OHM, 1/2 W, 5% TOL

Figure 5-15. NCU and CIE MD2 Board, Parts Layout Diagram and Parts List

In the CIE configuration the MD1 Board has the following options implemented:

a. RAM is used for microprogram memory. The PROM locations (E5, E7, and E9) on the MD1 Board must be vacant. The RAM is external to the MD1 Board and exists in the form of three separate boards referred to as the 7PM Boards, or CIE Control Memory Boards, described in paragraph 5.2.4 of this manual. This external RAM provides 4K words (12 bits each) of instruction memory and thus requires that the MPCR and AMPCR be implemented accordingly.

b. The MPCR is configured for 12 bits. Only the MPCR chip at location C3 is removed. See Figure 5-12, sheet 4, and Figure 5-13.

c. The AMPCR is configured for 16 bits and all AMPCR chips are in place. See Figure 5-12, sheet 4, and Figure 5-13.

d. The Selector chips are configured for 12 bits, and only the selector chip in location A3 is removed. See Figure 5-12, sheet 4, and Figure 5-13.

e. The jumper is not installed between pin 3 of B3 and pin 12 of B5. See Figure 5-12, sheet 4.

f. The SKIP 2 is enabled by a connection between pin 10 of E1 and pin 1 of E1, and the jumper is not installed from pin 10 of E1 to ground.

From the above paragraphs, it is obvious that the MD1 Boards are uniquely configured for NCU and CIE use and cannot be interchanged without reconfiguration. Hence, separate part numbers are assigned to these two configurations:

Part No.	Description
2600-5538	MD1 configured for CIE
2600-5538M	MD1 configured for NCU

It should be noted, however, that the MD2 boards used for NCU and CIE operation are identically configured and can be interchanged without modification. The MD2 Board is defined by Figure 5-14, sheets 1 through 5, and by Figure 5-15.

5.2.3.2 Functional Organization

The functional organization of the B7* is shown in Figures 5-5 and 5-6.

The Microprogram Memory (MPM) can be either:

a. 256 words (12 bits each) of PROM plugged into the three sockets E5, E7, and E9 on the MD1 Board. This is the case when the B7* is used as an NCU.

b. 4K words (12 bits each) of RAM on separate external cards which are interconnected with the MD1 card via the backplane. This is the case when the B7* is used as CIE.

The Memory Control Unit controls the addressing of program memory. Contained in this area are the Micro Program Count Register (MPCR) and the Alternate Micro Program Count Register (AMPCR). MPCR contains the address of the current MPM location being addressed. AMPCR usually contains a jump address for return from subroutines, but when not required for this prupose, AMPCR can be used by the Logic Unit as a scratch pad register.

The Control Unit performs condition selection and testing, successor determination, instruction register decoding, and timing control as described below:

The Condition Selection and Testing logic serves the following purposes:

a. The adjustment and testing of local condition flip-flops (LC1, 2, 3). These flip-flops are used as required by the programmer.

b. The external interrupt input (EXT) is used by an external source to provide a soft interrupt to the processor.

c. The Arithmetic Logic Unit (ALU) operation condition flip-flops are used to record the adder output results of the last Logic Unit Operation (LUOP), as follows:

FF	Meaning When Set
LST	Least significant bit was true.
MST	Most significant bit was true,
AOV	The operation resulted in an adder overflow (most significant carry).
ABT	The operation resulted in an all-ones output from the adder.

The successor determination logic is used during a Condition Test Operation (CTOP). All other operations result is an unconditional step. The possible successors are STEP, JUMP, SKIP 2, or EXECUTE and are based upon the condition selected by the CTOP instruction.

The Instruction Register is a 12-bit register and is loaded with the instruction data read from MPM. The Instruction Register contains the instruction currently being performed while the next instruction is being read from MPM, thus providing an EXECUTE-FETCH overlap feature.

The instruction decoding logic decodes the contents of the Instruction Register in preparation for instruction execution. Instruction decoding is accomplished in the first clock period following the Instruction Register load.

Figures 5-7, 5-8 and 5-9 illustrate typical timing sequences for various B7* instructions. Basically there are two types of instructions: Those which are performed serially (Type I) and those which are performed in parallel (Type II). Type I instructions include Logic Unit Operations and LITERAL-TO-DEVICE operations; all other instructions are Type II.

Type I instructions require nine clock periods for completion. Type II instructions require three clock periods for decoding and execution plus as many additional clock periods as are required to fetch the next instruction. In a Type I instruction the fetch time of the next instruction is overlapped by the serial execution time of the current instruction.

Figure 5-7 illustrates the timing of Logic Unit or LIT-TO-DEVICE instructions. At time strobe 7 and clock (CPIN) the previous instruction is completed and the new instruction is simultaneously loaded into the Instruction Register. The interval of time strobe P (Preset) is used to decode the contents of the Instruction Register in preparation for execution which is performed during time strobes 0 through 7, updating the Program Counter (MPCR) is accomplished at the clock of preset strobe and is always an increment (step) for Logic Unit or LIT-TO-DEVICE instructions.

In the single instruction mode, the B7* will perform one instruction each time the RUN line is pulsed. The instruction being performed is suspended in the last clock period of its execution. Upon reception of the next RUN pulse, the instruction held in suspension is completed, a new instruction is loaded into the instruction register, and that instruction is performed up to the final clock where it is then held in suspension awaiting the next RUN pulse.

5.2.3.3 Functional Description

Processor operations are carried out by the sequential exectuion of micro instructions. Each micro instruction is read from the program memory on the instruction cycle preceding its execution. The execution of each instruction is begun by loading that instruction into the Instruction Register. In the next clock period (preset strobe) the newly loaded instruction is decoded. The succeeding clock periods of the instruction cycle will then be used to execute the decoded instruction. Upon completion of the execution portion, the next instruction will be loaded into the Instruction Register and the sequence described above is repeated. Figure 5-10 defines the instruction set of the B7*.

As shown in Figure 5-10, there are three categories of instructions: namely, Literal instructions, Logic Unit instructions, and Condition Test instructions.

5.2.3.3.1 Literal Instructions

Bits 9 through 12 of the Literal instruction are used to decode the functional operation of the instruction. Bits 1 through 8 represent a binary number (Literal) to be loaded into the register as specified by the decoding. The following types of literal instructions are used:

a. Lit-to-Device Instructions (DEV 0, 1, 2, 3)

   The purpose of this instruction is to transfer the literal portion of the instruction to a particular register in the user's logic. A LITERAL-TO-DEVICE instruction is decoded when instruction bits 11 and 12 are both zero. Further decoding (that of DEV 0, 1, 2, or 3) is defined by instruction bits 9 and 10. These bits are decoded by the user to specify the particular register to be loaded.

b. LIT-TO-IR Instructions

The LIT-TO-IR (Literal to Instruction Register) instruction must precede the CALL or GOTO instruction if the AMPCR and MPCR are greater than 8 bits wide. The LIT-TO-IR instruction is used to load the most significant byte of the GOTO or CALL address into the Instruction Register for temporary storage while the CALL or GOTO instruction containing the least significant address byte is fetched. The CALL or GOTO instruction will load only into bits 9 through 12 of the Instruction Register thus leaving Instruction Register bits 1 through 8 (most significant address byte) unchanged and thereby permitting the concatenation of Instruction Register bits 1 through 8 with memory output bits 1 through 8 to make up a 16-bit CALL or GOTO address.

c. Call Instructions

As implied in the previous paragraph a CALL instruction with an address greater than 8 bits can be accomplished by performing two successive instructions, namely:

1. LIT-TO-IR (Fetch and hold most significant call address byte).

2. CALL (Fetch least significant call address byte and execute call).

The address bytes of these two instructions are concatenated and placed 16 bits parallel into the MPCR and at the same time the last previous contents of the MPCR are incremented and placed into the AMPCR as a return address.

If the widths of the AMPCR and the MPCR are not greater than 8 bits, a CALL or GOTO need not be preceded by a LIT-TO-IR instruction.

d. GOTO Instructions

A GOTO instruction of greater than 8 bits is accomplished by two successive instructions, namely: (1) LIT-TO-IR and, (2) GOTO. The address bytes of the two instructions are concatenated and placed 16 bits parallel into the MPCR. The contents of the AMPCR are not changed.

e. LIT-TO-B Instructions

The LIT-TO-B (Literal-To B-Register) instruction is decoded when bits 9 through 12 equal binary 1011, respectively. This will result in Instruction Register bits 1 to 8 being parallel transferred into the B-Register. The MPCR is incremented and the instruction is complete.

5.2.3.3.2 Logic Unit Instructions (LUOP)

A LUOP instruction is decoded when Instruction Register bits 11 and 12 are a binary 0 and 1, respectively. A LUOP will always result in a STEP (MPCR increment);

no other successor is possible. The formats and definitions of the Instruction Register bits are defined in Table 5-1 and in the following paragraphs:

Table 5-1. Format of Logic Unit Instruction

```
        Instruction Register Bits
       |-------------------------|
        1 2 3 4 5 6 7 8 9 10 11 12
       ---------------------------
       | X | OP + Y| Dest.  | 0 1 |
       ---------------------------
          |    |         |      |
          |    |         |      |
          |    |         |      |
          |    |         |      L------------------------ Command Code
          |    |         L---------------------- Destination
          |    L-- Operation and Y Select @
   X Select

   00  0        0000  X+B+1                  0000  B
   00  A1       0001  X+B                    0001  A1
   10  A2      *0010  X+Z+1                  0010  A2
   11  A3      *0011  X+Z                    0011  A3

                                 --
                0100  X EQV B (XBVXB)        0100  OUT 0
                                 - -
                0101  X XOR B (XBVXB)        0101  OUT 1
                0110  X-B (X+B+1)            0110  OUT 2
                          -
                0111  X-B-1 (X+B)            0111  AMPCR,  OUT 3
                           ---
                1000  X NOR B (XVB)         #1000  B, BEX  0
                           --
                1001  X NAN B (XB)          #1001  A1, BEX  1
                           ---
               *1010  X NOR Z (XVZ)         #1010  A2, BEX  2
                           --
               *1011  X NAN Z (XZ)          #1011  A3, BEX  3
                1100  X OR B (XVB)          %1100  B S
                1101  X AND B (XB)          %1101  A1 S
                             -
                1110  X RIM B (XVB)         %1110  A2 S
                             -
                1111  X NIM B (XB)           1111  A3, AMCPR
```

* Z = AMPCR. When AMPCR is not selected as a destination, then AMPCR will be "zero" (i.e., Z = 0) in all operations as a Y-Select input.

@ Y-SELECT = B or Z as indicated.

BEX indicates serial transfer from external register to B-Register while Adder transfers to other specified register (if B, then two inputs are ORed).

% S indicates a one-bit right shift of the destination register end off, with the MSB being filled by the Adder output.

The Logic Unit instruction specifies the Adder inputs, the operation, and the destination specifications for the Adder. The X-Select to the input of the Adder is either none or one of the three A-Registers (specified by bits 1 and 2). The operation and Y-Select to the input of the Adder are specified by bits 3, 4, 5, and 6 and include both arithmetic and logic operations on both the AMPCR and B-Register as indicated. The destinations of the Adder output as shown are specified by bits 7, 8, 9, and 10. The output of the Adder can go to B, A1, A2, or A3. The Adder output always goes to the external interface when a logic operation is selected, but if any OUT is selected as a destination, then a special 4-bit code is generated on the external control lines to enable gating from the adder to the particular external register. Of course, this is true only if the external interface is designed to perform this function. Note that if any of the BEX destinations are selected, a 4-bit selection code is sent out on the external control lines thus enabling an 8-bit serial transfer from the selected external register to the B-Register to take place in parallel with the Adder output into the specified register (i.e., A1, A2, A3, B). If the destination register is B, BEX, then an OR of the Adder output and the external input is performed. Normally, the Adder output in this case would be set to transfer zeros from the Adder, thereby allowing a simple external load of the B-Register.

As noted by *, if the AMPCR is not selected as the destination register, then the four operations using AMPCR as a Y-Select will have ZERO for a Y-Input. This means operations using AMPCR as a Y-Select can only be transferred back to AMPCR or A3. Through the use of this feature 0, 0-NOT, X and X-NOT can be transferred to any destination register except the AMPCR.

The destinations with S (for shift) allow the destinations to be shifted right end-off by one bit, and the most significant bit is supplied by the adder operating on the least significant bit of the X and Y selected operands. It should be noted that the Adder operation is performed on all eight bits of the input operands; the Adder condition bits (LST, MST, ABT, AOV) are set accordingly.

If one wishes to perform a right shift (end-off) of one bit on the B destination, then select (X=0, X+B, B,S) for the instruction. The primary purpose of the shift of the destination is to achieve right and circular shifts on A1, A2, and B, but all other allowed functions are valid into the destination's most significant bit. If the X=A1, X+B, A1,S) instruction is used, the addition takes place on bit 8 of both A and B, and the resulting bit is placed into bit 1 (MSB) of A11. Thereafter, bit 7 (LSB+1) of A1 is added to all bits of B, and the side effects on the Adder condition bits result accordingly. The last noteworthy side effect of a serial implementation of the Adder is that the Adder Overflow (AOV) condition is actually the initial and intermediate carry flip-flop for the serial Adder. As such, whenever a +1 operation is called for, the initial carry is set. In fact, the initial carry is set whenever bit 6 of the operation and Y-select field is zero. However, the initial carry flip-flop is enabled for intermediate carries only on arithmetic functions. For example, on an X OR B operation, bit 6 is zero, therefore AOV is set and remains set until a subsequent Logic Unit operation changes it.

5.2.3.3.3 Condition Test Instructions (CTOP)

A CTOP is decoded when Instruction Register bits 10, 11, and 12 are all ones. The remaining bits (1 through 9) are decoded as follows:

CTOP Bits	Function
1-3	Selects the condition to be selected.
4-5	Controls the set operation of the local condition flip-flops.
6-7	Selects the successor (STEP, JUMP, SKIP 2, or EXEC) if selected condition is true.
8-9	Selects the successor (STEP, JUMP, SKIP 2, or EXEC) if selected condition is false.

The following is a brief description of each of the selectable conditions:

a. MST, AOV, LST, ABT - These conditions reflect the results (Adder output) of the last LUOP:

   MST - Most significant bit was true.

   AOV - Adder overflow (most significant carry).

   LST - Least significant bit was true.

   ABT - All bits true (Adder result was all ones).

b. LC1, LC2, LC3 - These are local condition flags that are set by program control (see next paragraph) and are reset when tested.

c. Local Conditions Set Control - As described earlier, the set function for local condition flip-flops is controlled by instruction bits 4 and 5 of a CTOP. The set function specified by bits 4 and 5 will only occur if the test condition selected by bits 1, 2, and 3 is true.

   Example 1: IF LC1 THEN SET LC1 SKIP ELSE JUMP.
   This instruction will not change the state of LC1. If it is set it will remain set. If LC1 is not set, it will remain reset.

   Example 2: IF LC1 THEN STEP ELSE SKIP.
   This instruction will always reset LC1 after testing it.

   Example 3: IF MST THEN SET LC1 STEP ELSE STEP.
   This instruction will set LC1 if MST = 1 otherwise LC1 will be left unchanged.

d. Successor Select - Successor selection is specified by instruction bits 6, 7, 8, and 9 of a CTOP. Bits 6 and 7 specify the successor if the condition selected by bits 1, 2, and 3 is true; however, is the selected condition is false, then bits 8 and 9 will specify the successor. An unconditional successor is specified by selecting the same successor for the true and false condition. The possible successor selections are:

STEP - MPCR is incremented, thus the next instruction will be fetched from the micro program memory at the next sequential address.

JUMP - A copy of the contents of AMPCR is loaded into MPCR. The previous contents of MPCR is discarded. Thus, the next instruction fetched from the micro program memory will be at the address specified by MPCR, which now is the same as AMPCR.

SKIP - For B7* machines, where MPCR and AMPCR are only 8 bits wide, the MPCR is incremented twice. Thus, the next instruction is fetched from the micro program at the current address +2.

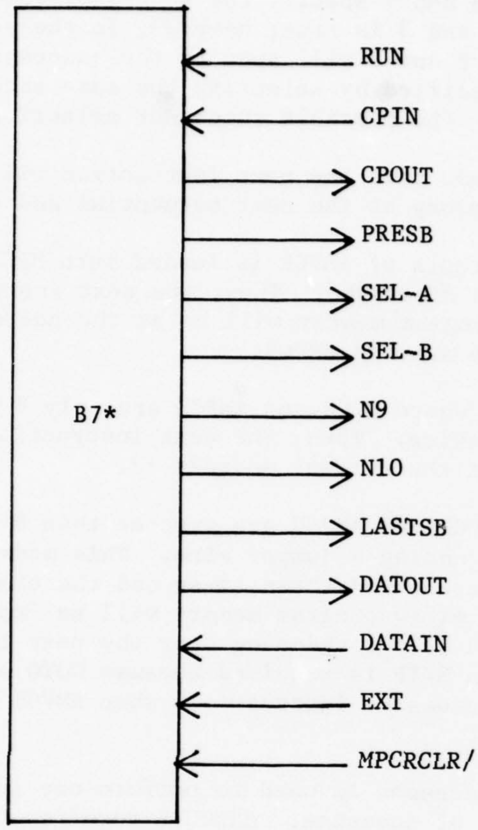
For B7* machines where MPCR and AMPCR are greater than 8 bits wide, SKIP will be modified by adding a jumper wire. This modification will cause MPCR to be incremented three times and therefore the next instruction fetched from micro program memory will be from the current address +3. This feature allows skipping over the next two instructions. A two-instruction SKIP is required because GOTO and CALL functions require two successive instructions when AMPCR and MPCR are greater than 8 bits wide.

EXECUTE - The EXECUTE successor is used to perform one instruction (specified by AMPCR) out of sequence. EXECUTE requires two instruction periods for completion. The first instruction period will increment MPCR, swap the contents of AMPCR and MPCR, and then fetch the instruction per MPCR (originally AMPCR). The second instruction period will execute the instruction fetched above, increment MPCR, again swap the contents of AMPCR and MPCR, and fetch the instruction specified by MPCR.

In summary, an EXECUTE will perform the instruction specified by AMPCR and increment both AMPCR and MPCR.

5.2.3.4 Interface Requirements

The physical interconnections for the two cards constituting the B7* MINI-D processor are shown in Figure 5-11. The diagram below depicts the B7* user's interface. Signals ending with a slash (/) are low-true; absence of a slash implies high-true. All signals are directly TTL compatible.



These signals are described below:

a. CPIN (Clock Pulses In) - This signal provides the basic clock to the B7*. It presents a load of two high-speed TTL loads and should be driven by a high-speed TTL device. Precaution should be taken as required to avoid ringing or noise on this line. Frequency of this input may range from 0 to 10 MHz. Pulse width can range from 24 nanoseconds to 50 percent of the clock period.

b. CPOUT (Clock Pulses Out) - The purpose of this signal is for the user to clock external data registers when transferring serial data to or from the B7* via the DATIN or DATOUT lines.

   CPOUT is identical to CPIN except that the clock pulse during PRESB is missing and CPOUT is delayed from CPIN by 15 to 34 nanoseconds. The drive capability of CPOUT is ten TTL loads.

c. PRESB (Preset Strobe) - This signal may be used to synchronize user logic to B7* instruction timing. PRESB represents the first clock period of each instruction. It is the decoding time of an instruction preceding execution. PRESB is one clock period in duration and is delayed from CPIN by 20 to 45 nanoseconds. PRESB has a drive capability of 5 TTL loads.

d. SEL-A, SEL-B, N9 and N10 - These signals control the serial data exchange between B7* and external (user's) logic.

SEL-A and SEL-B control the type of data exchange as shown below:

SEL A B	Description of Data Exchange
0 0	No Data Exchange
0 1	BEX (Transfer data from external logic to B7*'s ALU)
1 0	OUT (Transfer data from B7*'s ALU to external logic)
1 1	DEV (Transfer data from B7*'s I-Reg to external logic)

N9 and N10 select a particular port (path) in the external logic. Hence, the type of data exchange defined by SEL-A and SEL-B may be performed on port 0, 1, 2 or 3 as defined by N9 and N10.

SEL-A, SEL-B, N9, and N10 will switch during the first clock period of each instruction (PRESB) and will remain stable during the execution portion of each instruction.

N9, N10 can drive five TTL loads each. SEL-A and SEL-B can drive ten TTL loads each.

e. DATAOUT - DATAOUT is used to serially transfer data from the B7* to the user's logic. It is shifted into the user's logic during DEVN of a LUOP with an OUTN destination.

DATAOUT will switch (worst case) 20 nanoseconds prior to the trailing edge (positive-to-negative) transition of CPOUT and can drive seven TTL loads.

f. DATAIN - DATAIN is used to serially transfer data from the user's logic to the B7* Logic Unit B-Register. This transfer takes place during LUOP with BEX destination. DATAIN must be stable 40 nanoseconds prior to the trailing edge (positive-to-negative transition) of CPOUT. DATIN has a drive requirement of two TTL loads.

g. EXT (External Interrupt) - The EXT signal allows the user's logic to provide a soft interrupt to the B7*. It is examined by the B7* at the first clock period following PRESB of a CTOP, if EXT is the condition selected. EXT must not change during the clock period on which it is being examined. The drive requirement of EXT is one TTL load.

h. MPCRCLR/ (MPCR Clear/) - This line will clear MPCR to zero and can be used as a hard interrupt, i.e., unconditionally restart the program from step zero. The drive requirement is six TTL loads. MPCR should span at least one instruction period (nine clocks) or from one PRESB to the next.

i. LASTSB - This signal will be true during the last clock period of an instruction and will be extended whenever the B7* is stopped. It is provided for timing purposes in the user's logic and has a drive capability of four TTL loads.

j. RUN - The RUN line is at a high level for continuous operation. However, the line may be pulsed for single instruction execution.

5.2.4 CIE CONTROL MEMORY

The CIE Control, or Program, Memory provides read/write memory capability for 4K (K = 1024) words (12 bits/word) of instructions. That is, each instruction used by the CIE B7* is 12 bits long and occupies one control memory location. These 4K words are divided between two separate boards with each board providing storage for 2K words. The boards, part number 2601-1668M, are defined by the schematics of Figure 5-16, sheets 1 thru 7. The board layout is shown on Figure 5-17.

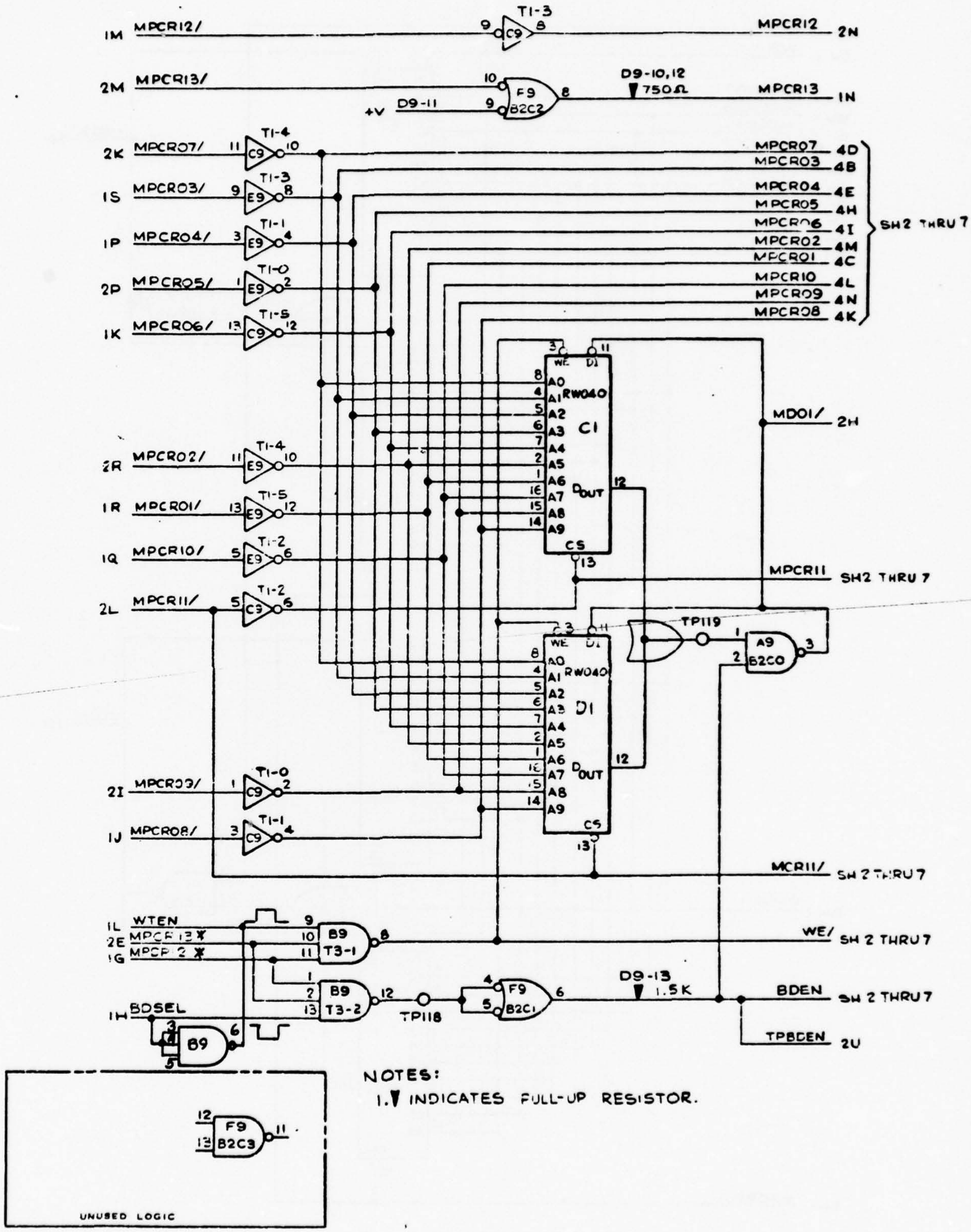
The Control Memory board design is based upon the use of NMOS static RAM chips (2102A's), each having the capacity of 1K bits. The chips are arranged on the board so that two adjacent memory chips (RW04's on Figure 5-16, sheets 1 through 7) are associated with each bit of the 12-bit instruction word. Hence, 12 sets (24 RW04 chips) provide for storing 2048 twelve-bit words. Two additional RW04 chips, at locations E1 and F1, provide capability for a parity bit per instruction word. This parity capability is not used, however, in the ESM application. The association of RW04 chip-pairs with specific instruction-word bit positions is apparent in Figure 5-16, sheets 1 through 7. That is, input/output lines for each chip-pair are labeled MD01' through MD12'; MD01' is the most significant bit and MD12' is the least significant bit of the instruction word.

5.2.4.1 Memory Addressing

CIE Control Memory addressing is accomplished from the Microprogram Count Register (MPCR) of the CIE B7* (MD1 Board). This address is fed to the Control Memory boards on lines MPCR01' through MPCR12'. Refer to Figure 5-16, sheet 1. MPCR01' represents the most significant bit of the address and MPCR12' represents the least significant bit of the address. The line labeled MPCR13' is not used since only 12 bits are required to access the 4K words of memory. Similarly, the line labeled MPCR13* is tied directly to V_{cc} via backplane wiring.

The lines labeled MPCR 12' and MPCR12* are connected together on the backplane for the first board (first 2K) only. The MPCR12' signal is inverted via C9, pins 9 and 8, and fed out of the first board at terminal 2N. This terminal is connected to terminal 1G (MPCR12*) of the second board (second 2K). Hence, when MPCR12' is high, a high is applied at pin 11 of B9 on the first board, allowing access to the first 2K. When MPCR12' is low, a high is applied at pin 11 of B9 on the second board, allowing access to the second 2K.

MPCR11' controls the Chip Select (CS) terminal of each RW04 chip. That is, when MPCR11' is high, the first chip (upper chip in the figures) of the two-chip pair is selected. This first chip represents the first 1K on the board selected by MPCR12' as described above. When MPCR11' is low, the second chip of the two-chip set (second 1K on the selected board) is selected.



NOTES:
1. ▼ INDICATES PULL-UP RESISTOR.

Figure 5-16. CIE Control Memory Logic (Sheet 1 of 7 Sheets)

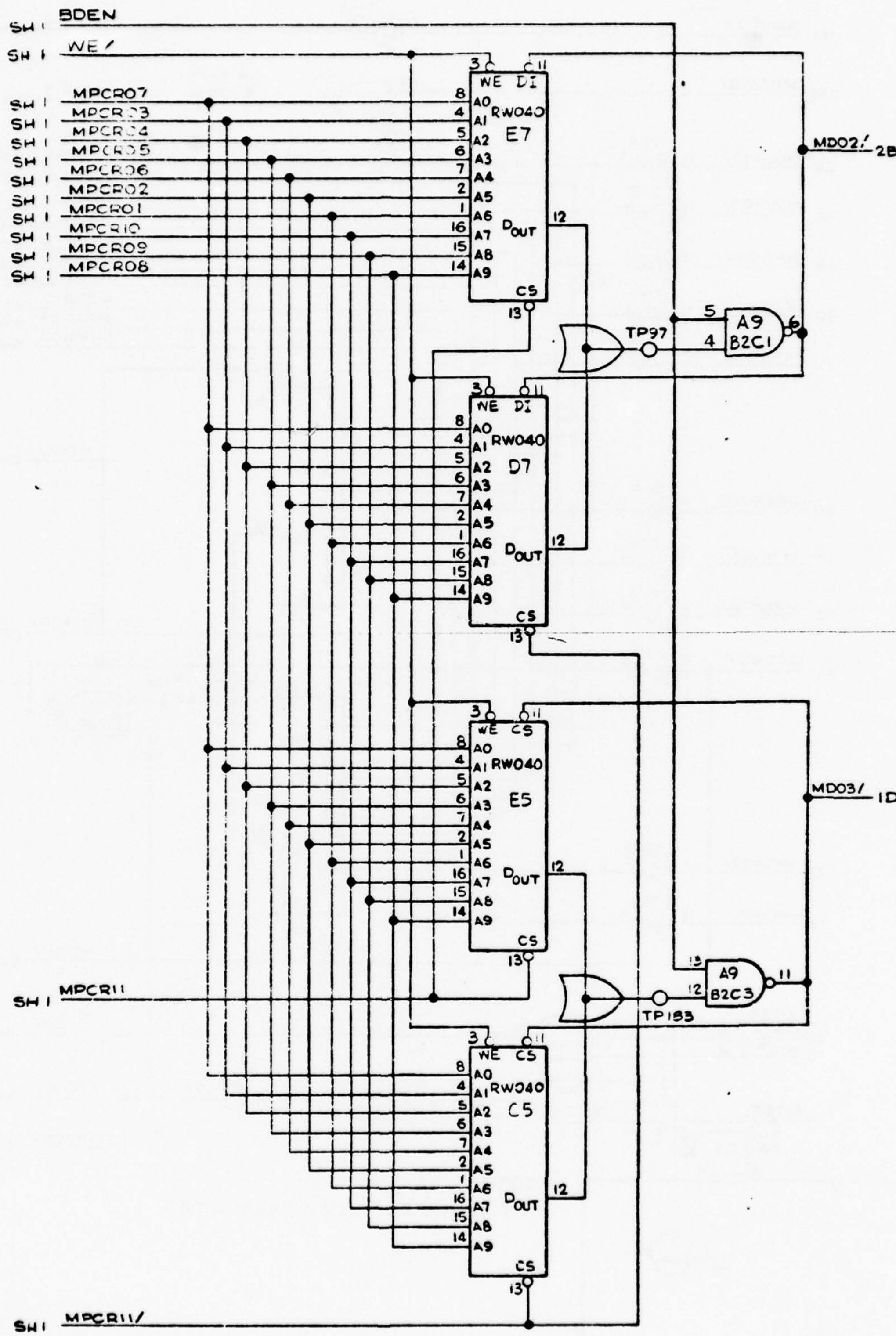


Figure 5-16. CIE Control Memory Logic (Sheet 2 of 7 Sheets)

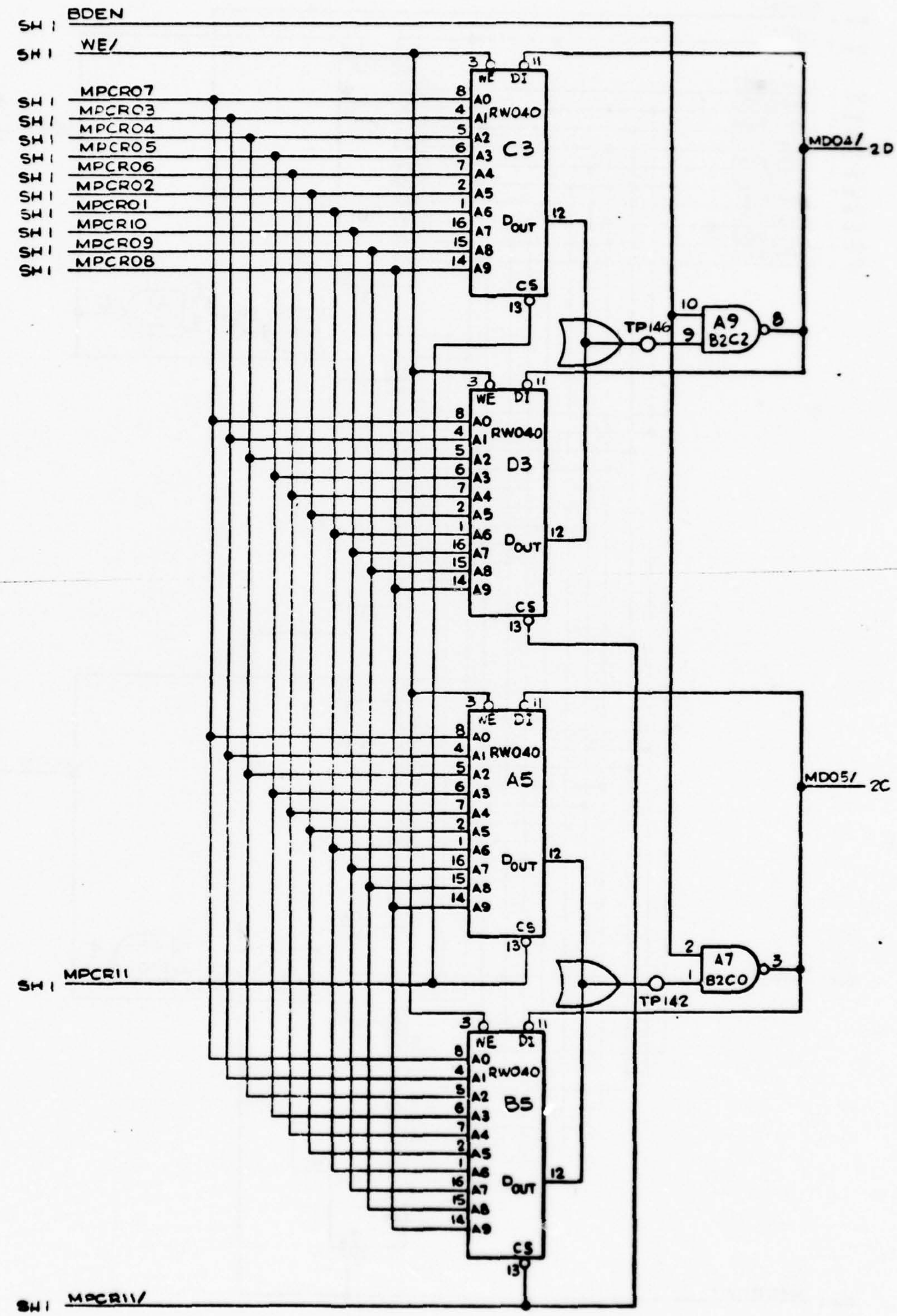


Figure 5-16. CIE Control Memory Logic (Sheet 3 of 7 Sheets)

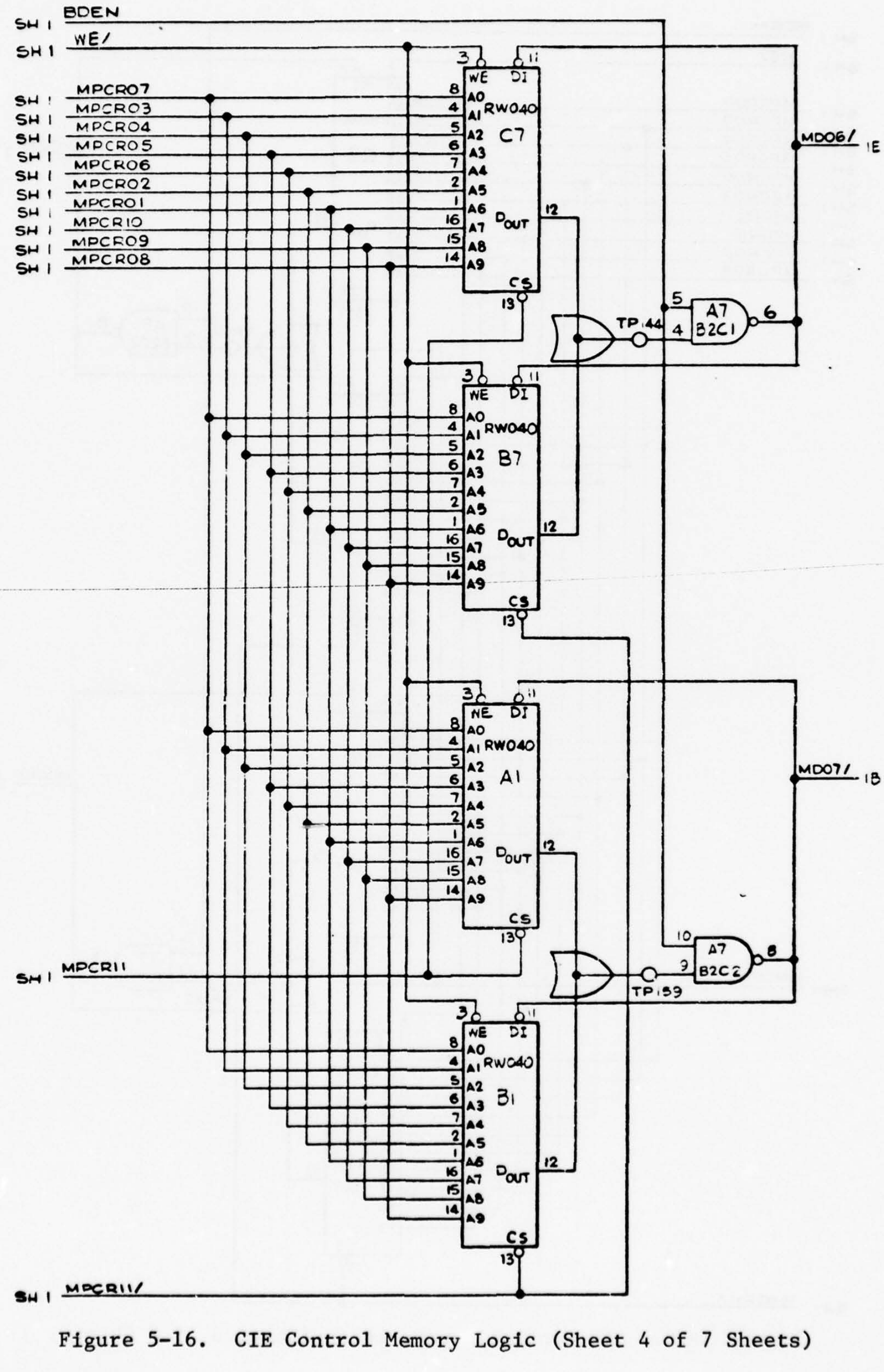


Figure 5-16. CIE Control Memory Logic (Sheet 4 of 7 Sheets)

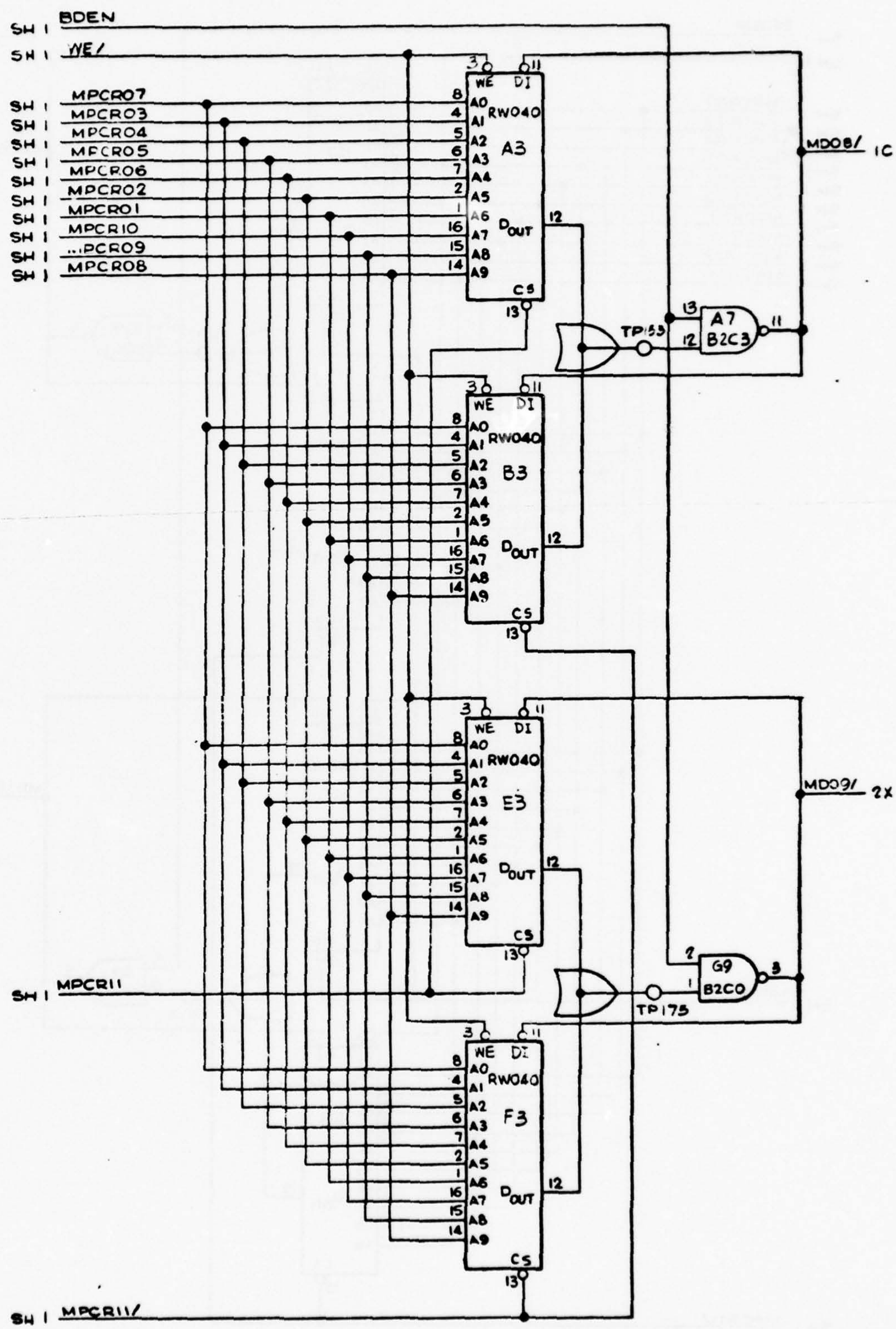


Figure 5-16. CIE Control Memory Logic (Sheet 5 of 7 Sheets)

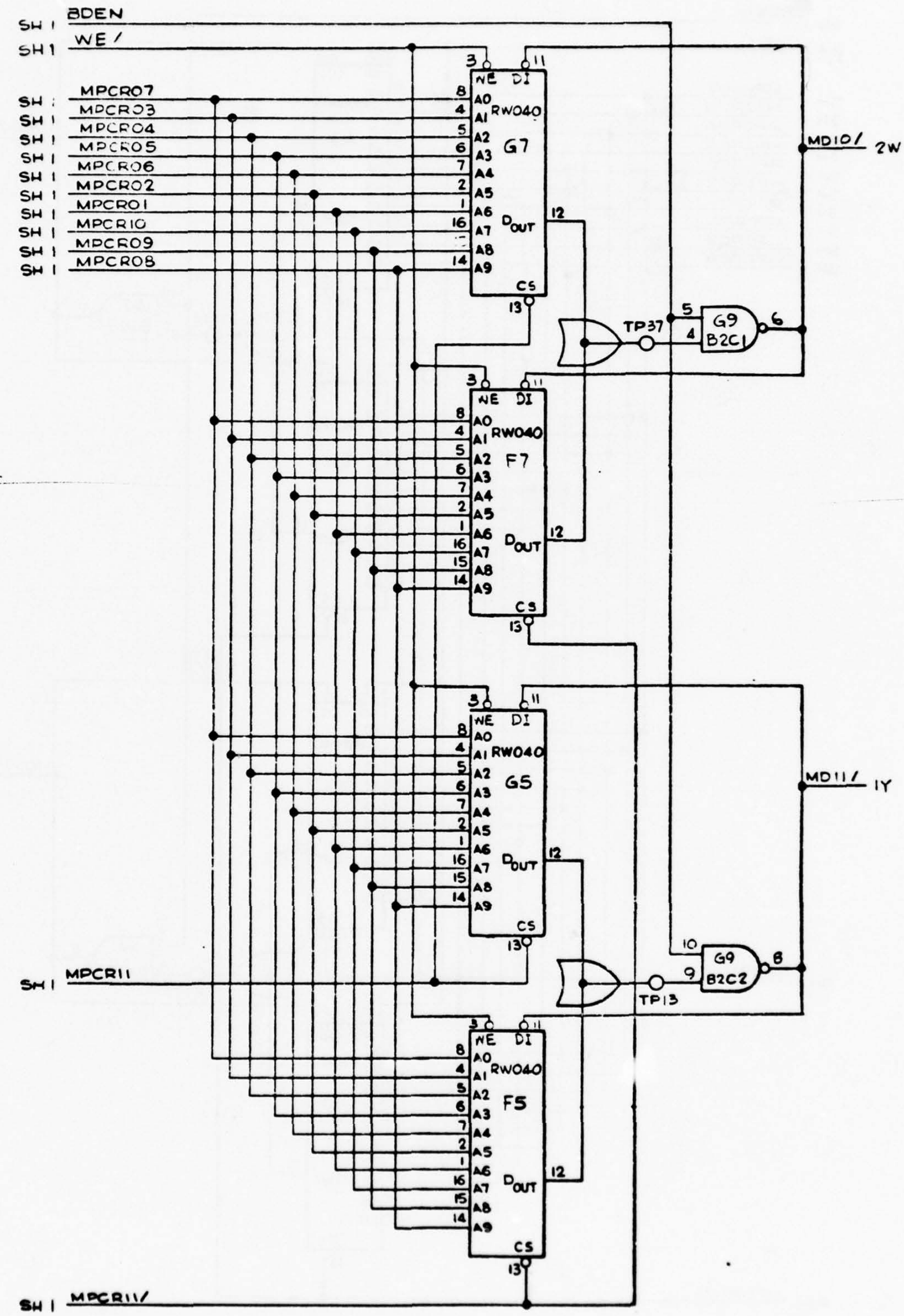


Figure 5-16. CIE Control Memory Logic (Sheet 6 of 7 Sheets)

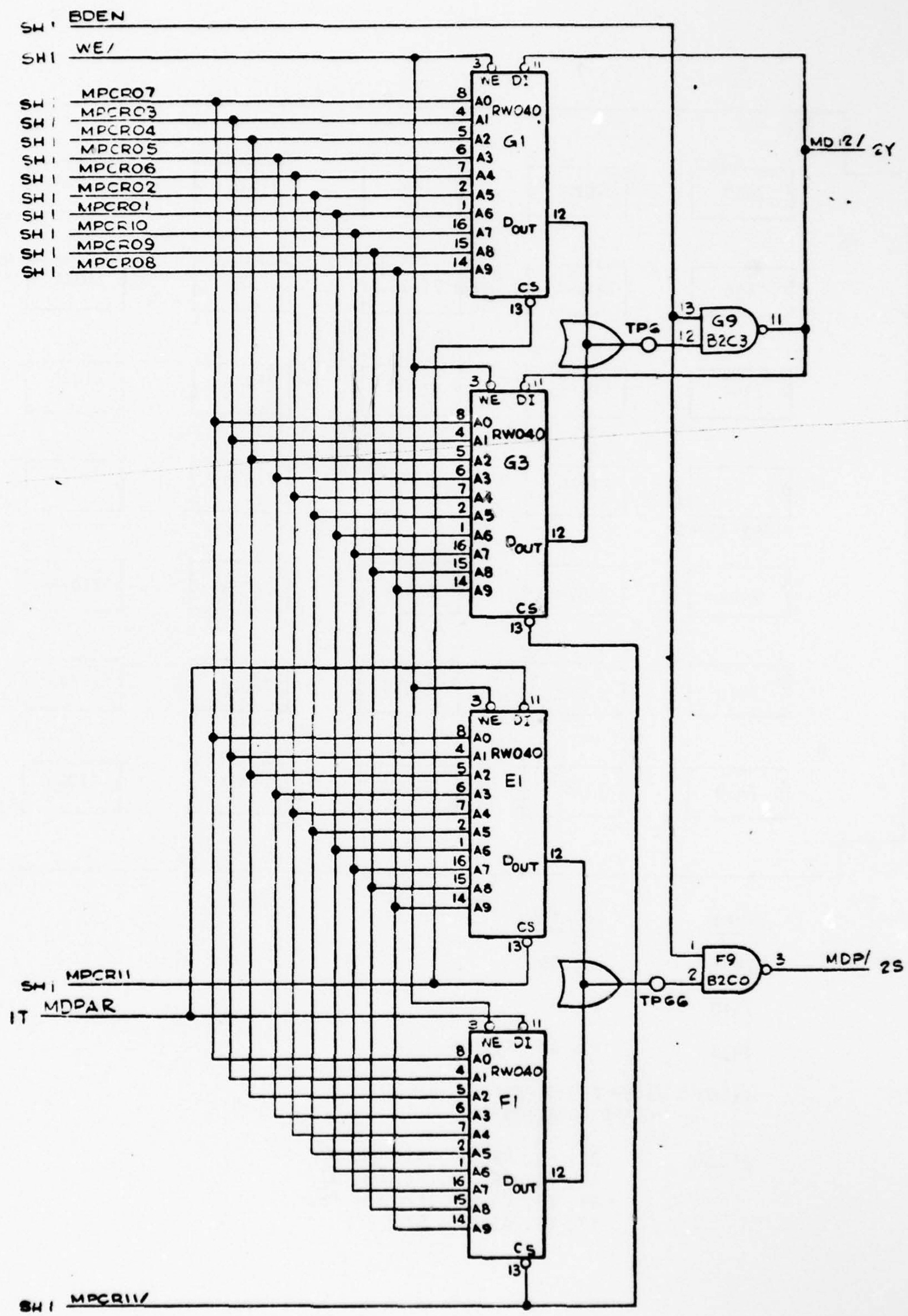
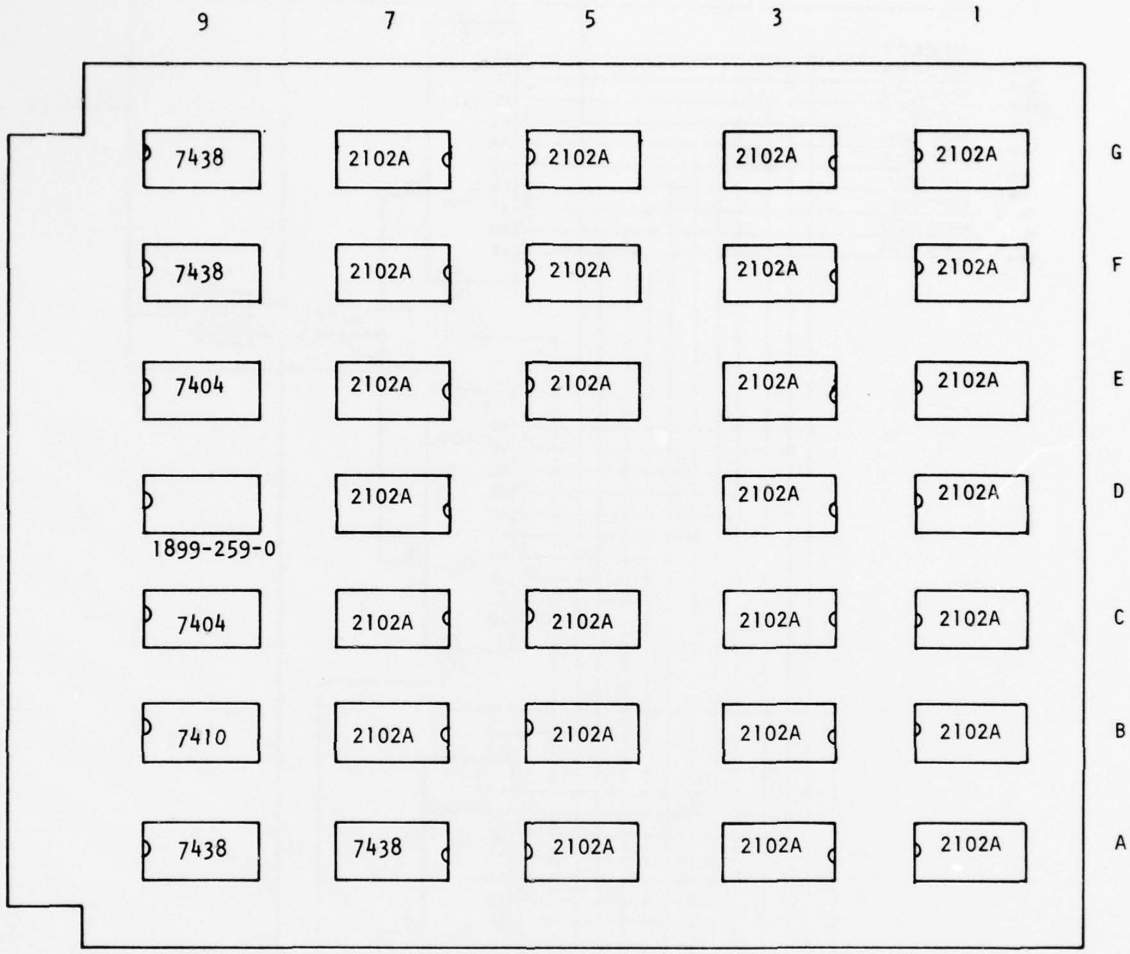


Figure 5-16. CIE Control Memory Logic (Sheet 7 of 7 Sheets)



IDENT	LOCATION
7404	C9, E9
7410	B9
7438	A7, A9, F9, G9
BECKMAN #1899-259-0 RESISTOR DIP, BOARD LOCATION D9	
2102A	A1, A3, A5, B1, B3, B5, B7, C1, C3, C5, C7, D1, D3, D7, E1, E3, E5, E7, F1, F3, F5, F7, G1, G3, G5, G7

Figure 5-17. CIE Control Memory Board, Parts Layout Diagram and Parts List

MPCR10' through MPCR01' select the specific bit address within each selected chip on the selected board. These ten lines allow accepting all 1024 bits per chip. When one or more of these lines go low, the corresponding bit location is addressed.

5.2.4.2 Data Input

Data input is via signal lines MD01' through MD12'. Input to control memory can only be from the Loader Board, refer to paragraph 5.2.13. MD01' represents the most significant bit and MD12' the least significant bit; MD13' is not used in the ESM. These same lines are also used for data output as described below. Data applied to these lines is routed to the input pins (pin 11) of the RW04 chips. This data is then written into the addressed location via a write pulse signal (low level) applied to the Write Enable pin (pin 3) of the RW04 chips.

The write pulse, which must be at least 250 nsecs (preferably 300 nsecs), is fed in from the Loader Board to terminal 1H of the memory boards. This signal, labeled BDSEL, is applied to pin 13 of B9. It is also inverted, via B9, pins 3-6, and applied to pin 9 of B9. This input is labeled WTEN. No external connection is made to this line at terminal 1L. The output from B9, pin 8, is a negative pulse which strobes the data on the data-in lines into the addressed location. An output from B9, pin 12, occurs at the same time. This output is inverted and applied to output gates on A9, A7, and G9 to inhibit data output from the addressed memory locations during write time. This signal is labeled BDEN. The required timing relationships of the various signals are shown in Table 5-2.

Table 5-2. RW04 (2102A) Chip Characteristics

Read Cycle - 350 nsecs minimum

a. Change address and/or chip enable

b. Data valid 350 nsecs later

c. Previous data invalid 0 nsec after chip enable changes

Write Cycle - 350 nsecs minimum

a. Change address and/or chip enable

b. Apply Data for duration of write pulse, or longer

c. Apply Write Pulse (250 nsecs minimum duration) a minimum of 20 nsecs after address change

d. Data written is valid after minimum duration of write pulse.

5.2.4.3 Data Output

Data output is via signal lines MD01' through MD12'. Output from control memory is only to the Instruction Register of the associated CIE B7*. MD01' represents the most significant bit and MD12' represents the least significant bit. MD13' is not used in the ESM. These same lines are used for data input as described above. When an address is applied (lines MPCR01' through MPCR12') and the level at the Write Enable input (pin 3) of the RW04 chips is high, the data bits (instruction) stored at the location appears on the Data Output pins (pin 12) of the addressed RW04 chips. Outputs from each two-chip pair are OR'ed together, but the output of only one of the two chips is active at any one time. Further, the output is active only when chip select is active (low), as determined by MPCR11'. The output is then routed to the appropriate MDXX' line via the gates of A7, A9, and G9. The gates are enabled by the externally applied Write Enable signal as explained above. That is, a high on the BDSEL line will result in these gates being enabled. The required timing relationships of the various signals are shown in Table 5-2.

The output lines for each of the 12-bits of the first board are tied to those of the second via the backplane. These open collector outputs are then routed to the Instruction Register inputs on the B7* MD1 Board. These outputs, which are also inputs during load-time, are also routed to the Loader Board. The pull-up resistors for these lines are included on the Loader Board.

5.2.5 DATA MEMORY

This section describes both the CIE Data Memory and the NCU Data Memory. The CIE Data Memory provides a read/write capability of 11K (K = 1024) bytes (8 bits byte) of data. This total of 11K bytes is divided among three separate PC boards. The first two boards (part number 2601-8929) each contain 4K bytes; the third board (part number 2601-8929M1) contains 3K bytes. The two board types are identical with the exception that 2601-8929M1 has one column (column 1) of memory chips (1K bytes worth) removed. This configuration is identified by Note [illegible] on Figure 5-18, sheet 1, and Note 1 on Figure 5-19. Also, 2601-8929M1 includes a ground tang for test use, per Note 2 on Figure 5-19.

NOTE

> Part number 2601-8929 can be used in place of part number 2601-8929M1 without any adverse effects. However, the memory chips in column 1 of the 2601-8929 board will never be accessed.

The NCU Data Memory provides read/write capability of 1K bytes of data, and is contained on a single PC board (part number 2601-8929M2). This PC board is identical to 2601-8929 except that:

a. Memory chips are removed from columns 3, 5 and 7.

b. Chip locations A9 and E9 are changed from 7438's (open collector outputs) to 7437's.

This configuration is defined by Note 4 on Figure 5-18, sheet 1, and on Figure 5-20.

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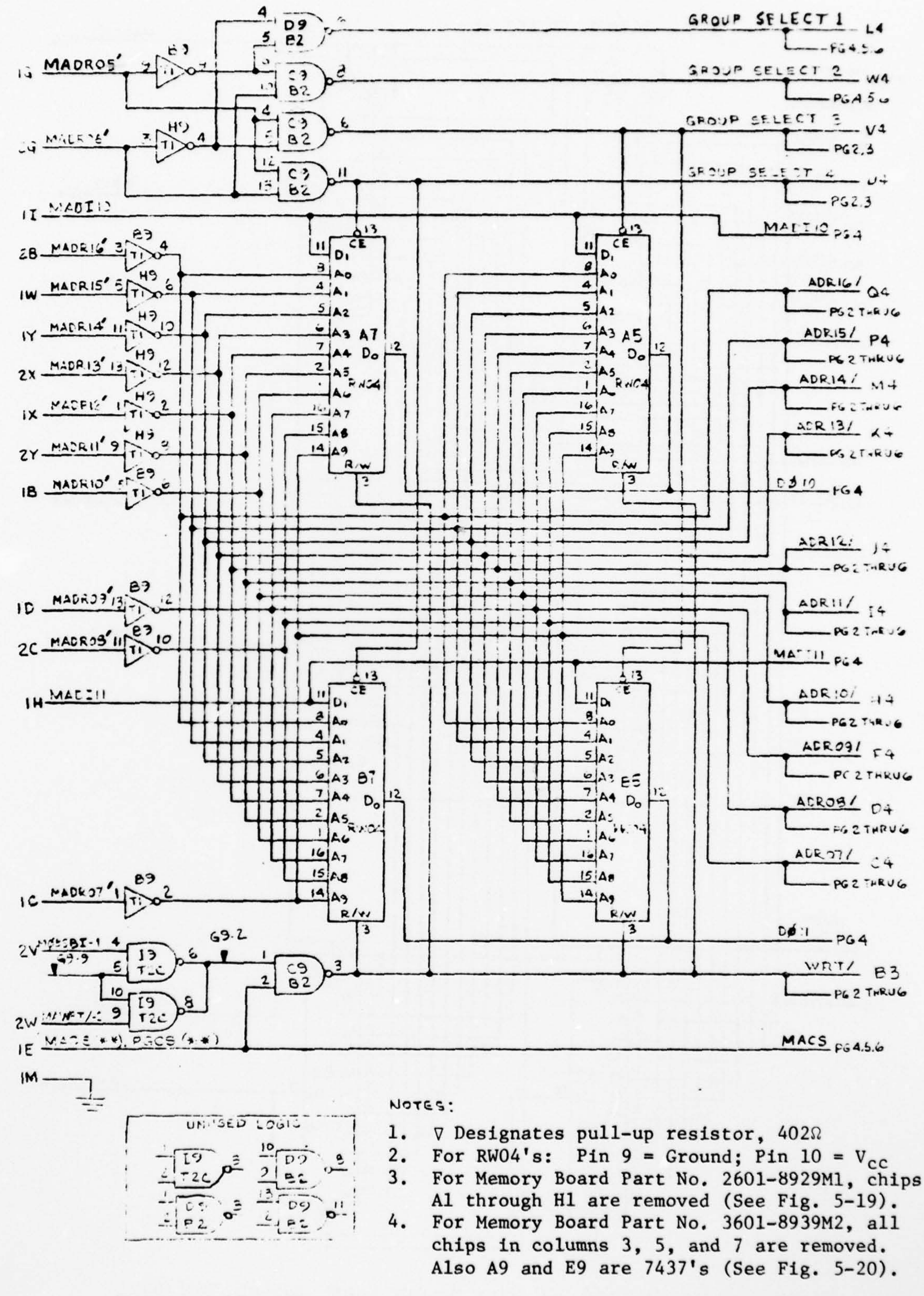


NOTES:

1. ∇ Designates pull-up resistor, 402Ω
2. For RW04's: Pin 9 = Ground; Pin 10 = V_{CC}
3. For Memory Board Part No. 2601-8929M1, chips A1 through H1 are removed (See Fig. 5-19).
4. For Memory Board Part No. 3601-8939M2, all chips in columns 3, 5, and 7 are removed. Also A9 and E9 are 7437's (See Fig. 5-20).

Figure 5-18. CIE and NCU Data Memory Logic (Sheet 1 of 6)

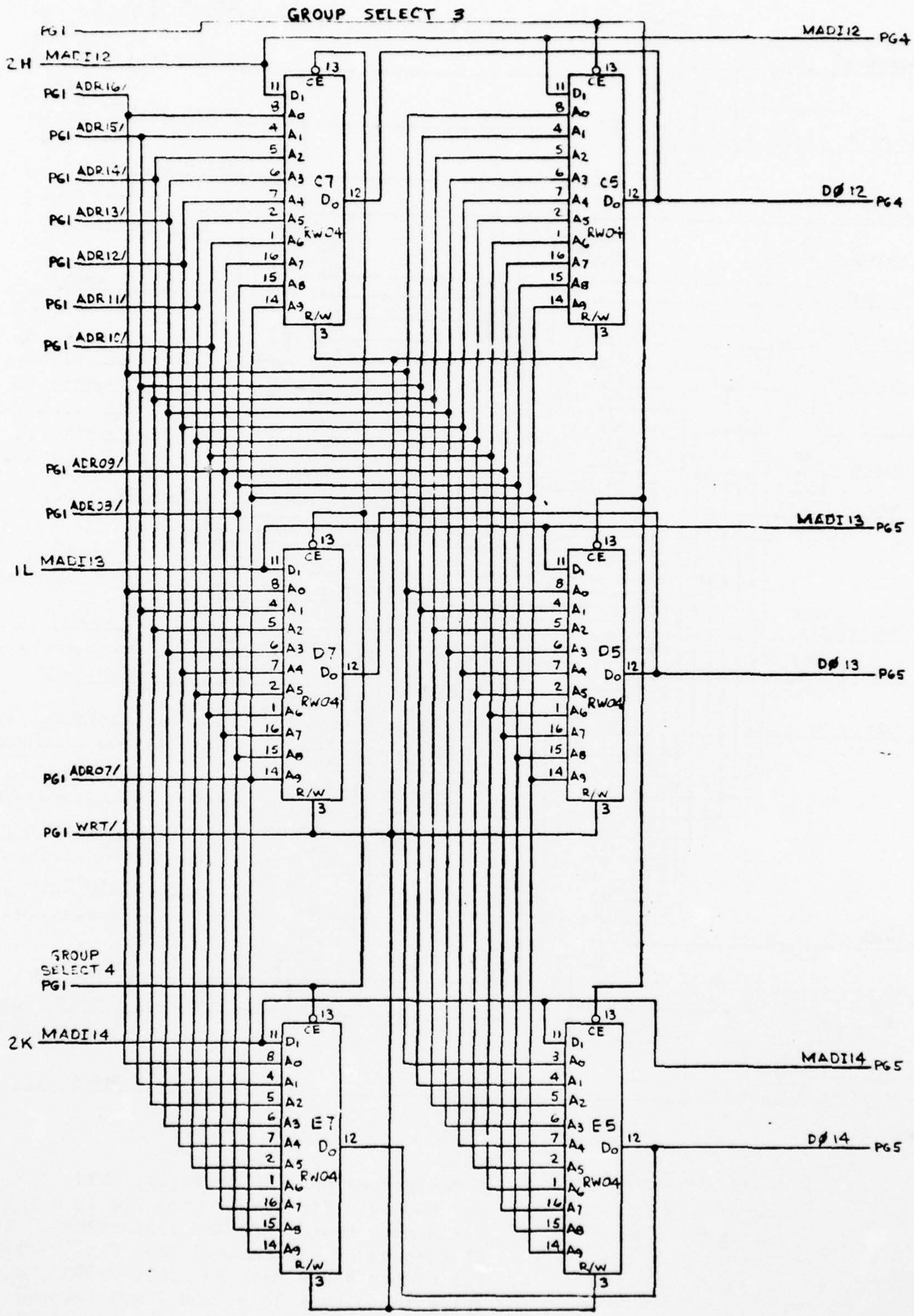


Figure 5-18. CIE and NCU Data Memory Logic (Sheet 2 of 6)

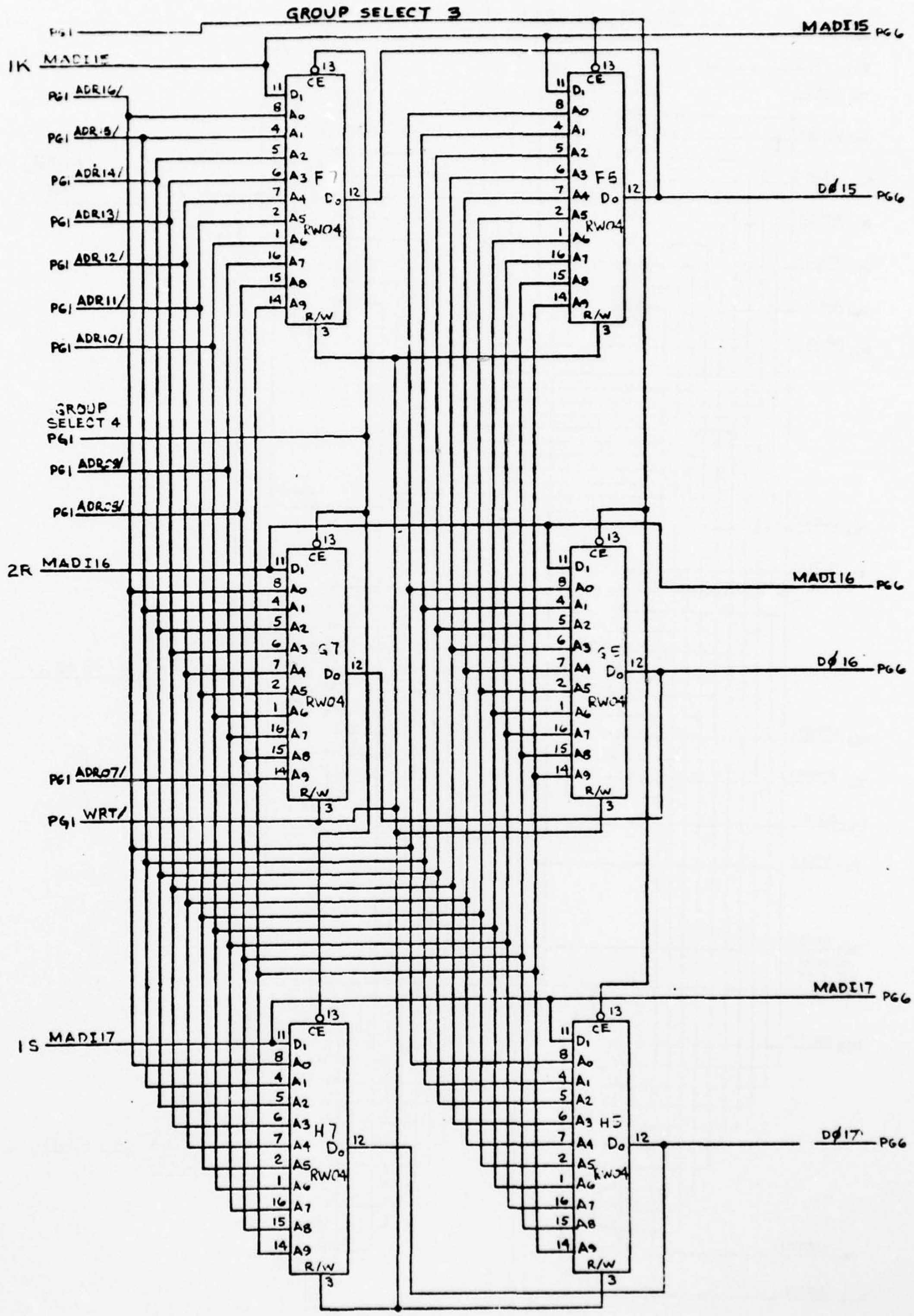


Figure 5-18. CIE and NCU Data Memory Logic (Sheet 3 of 6)

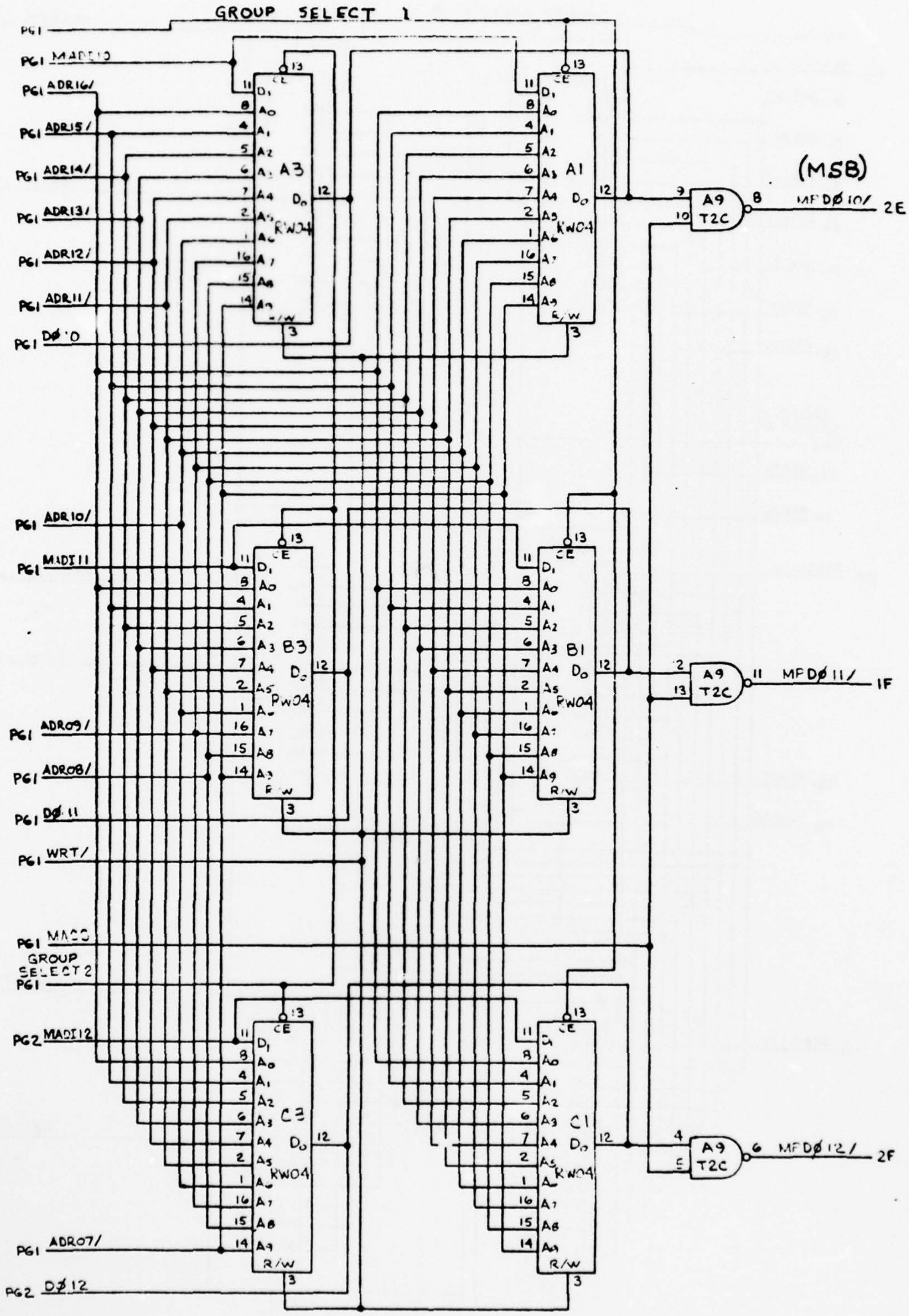


Figure 5-18. CIE and NCU Data Memory Logic (Sheet 4 of 6)

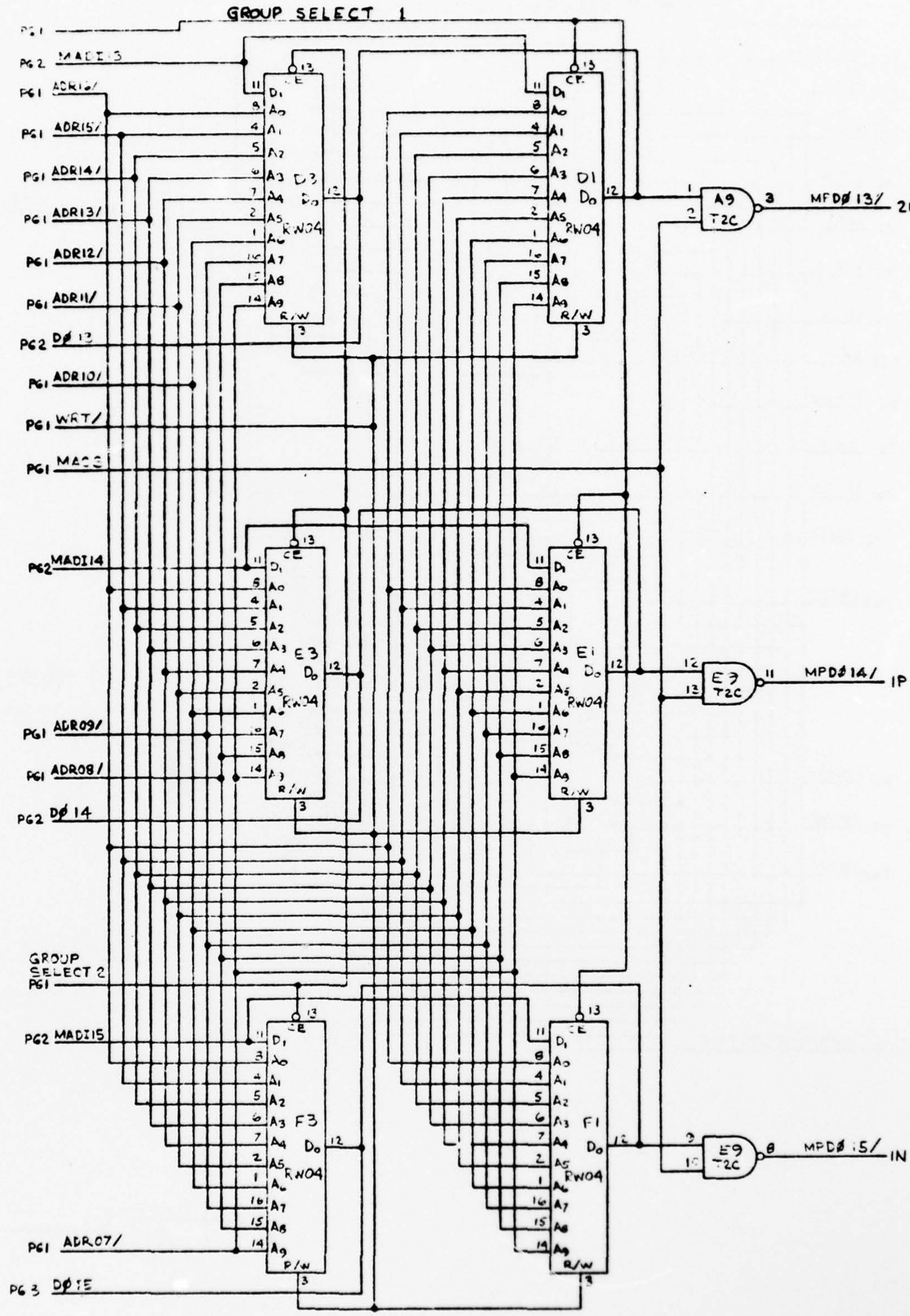


Figure 5-18. CIE and NCU Data Memory Logic (Sheet 5 of 6)

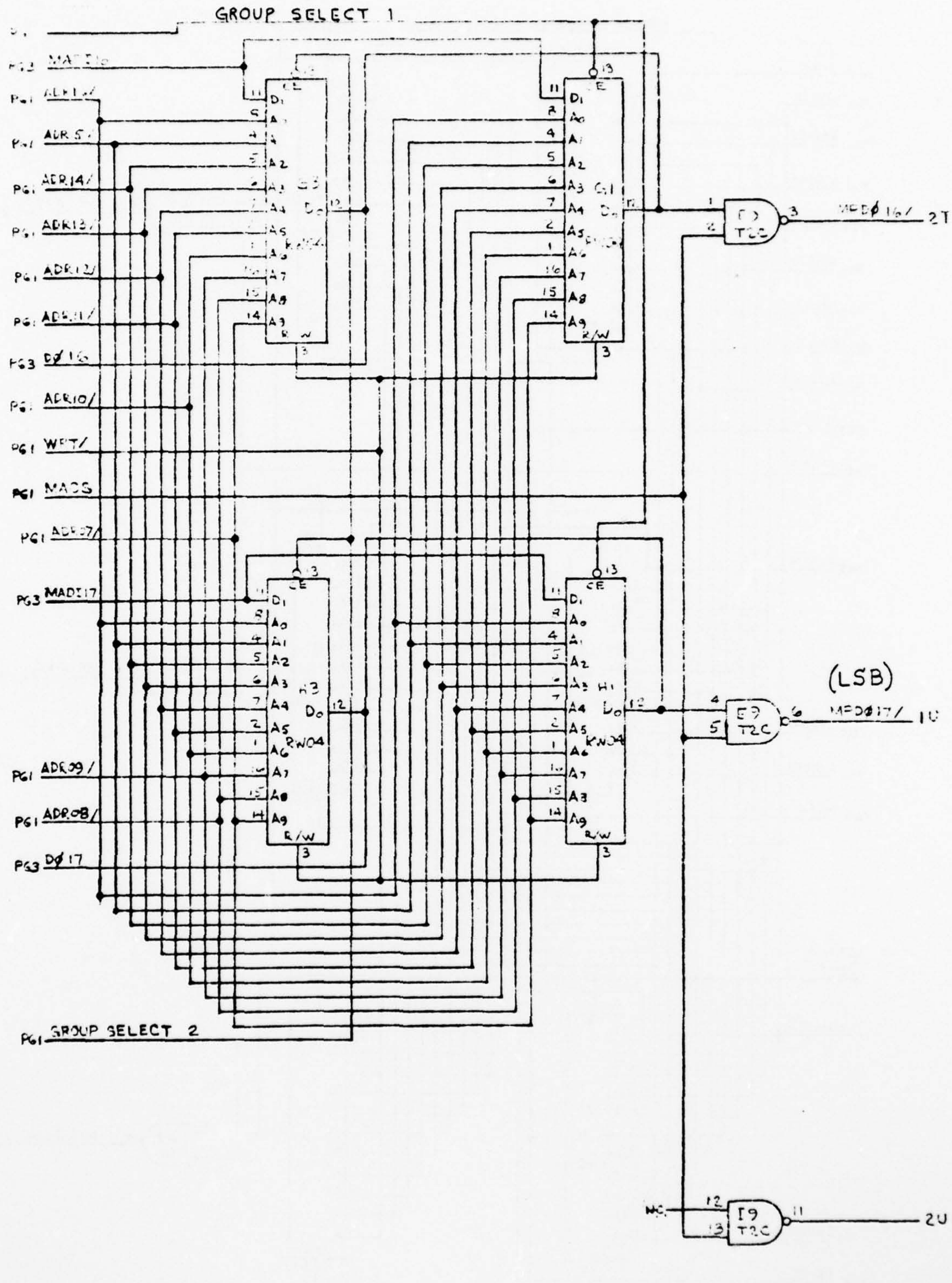
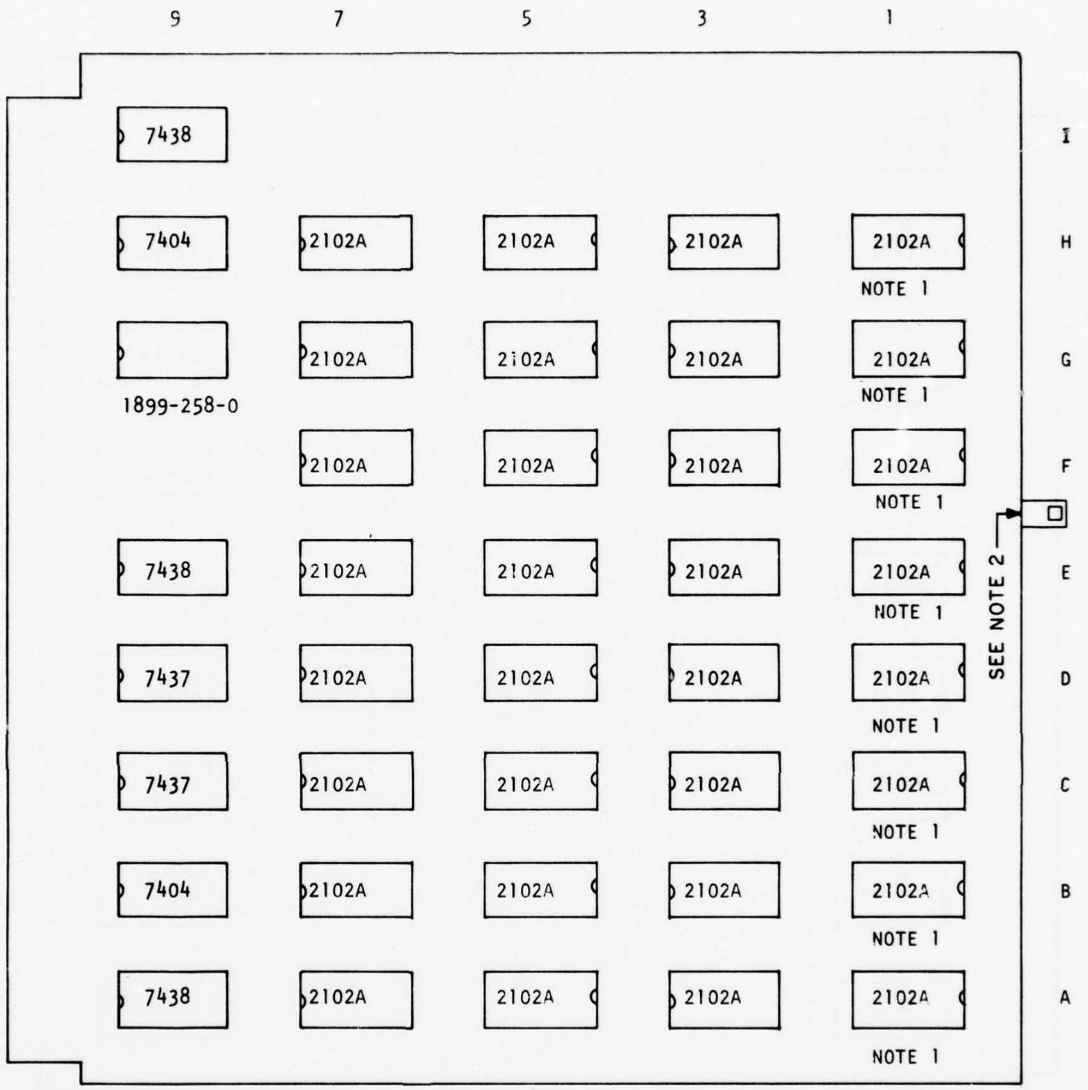


Figure 5-18. CIE and NCU Data Memory Logic (Sheet 6 of 6)



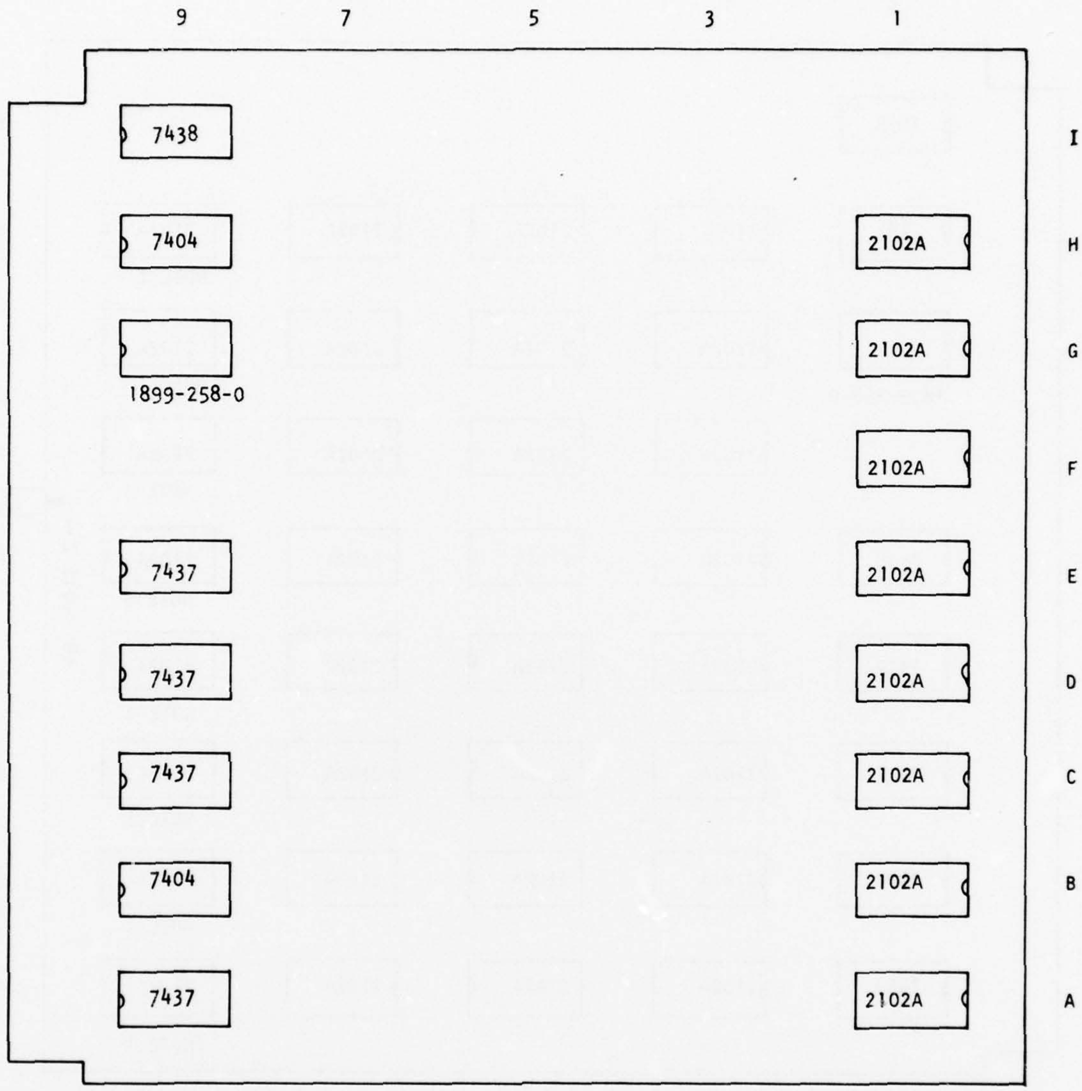
IDENT	LOCATION
7404	B9, [illegible]9
7437	C9, D9
7438	A9, E9, I9
BECKMAN #1899-258-0 RESISTOR DIP, BOARD LOCATION G9	
2102A	A1, A3, A5, A7, B1, B3, B5, B7, C1, C3, C5, C7, D1, D3, D5, D7, E1, E3, E5, E7, F1, F3, F5, F7, G1, G3, G5, G7, H1, H3, H5, H7

NOTES

ALL CHIPS APPLY TO CIE DATA MEMORY BOARDS #1, #2 & #3 UNLESS OTHERWISE NOTED.

1. EMPTY SOCKET ON CIE DATA MEMORY BOARD #3.
2. GROUNDED TANG FOR TEST USE, APPLIES ONLY TO CIE DATA MEMORY BOARD #3.

Figure 5-19. CIE Data Memory Board, Parts Layout Diagram and Parts List



IDENT	LOCATION
7404	B9, H9
7437	A9, C9, D9, E9
7438	I9
BECKMAN #1899-258-0 RESISTOR DIP, BOARD LOCATION G9	
2102A	A1, B1, C1, D1, E1, F1, G1, H1

Figure 5-20. NCU Data Memory Board, Parts Layout Diagram and Parts List

The memory board design is based upon the use of MOS Static RAM chips (2102A's) each having the capacity of 1K bits. The board is configured such that each column of 2102A-type chips on the board represents 1K bytes of storage. Column 1 is the first 1K, and column 7 the last 1K per board. Further, each of the eight rows of 2102A chips represents one bit of the 8-bit byte. Row A contains the most significant bit and row H contains the least significant bit. Refer to Figures 5-19 and 5-20.

5.2.5.1 Memory Addressing

CIE Memory addressing is accomplished from the CIE Ancillary Board, which is described in paragraph 5.2.7. NCU Data Memory addressing is accomplished by either the CIE Ancillary Board or the NCU Ancillary Board (see paragraph 5.2.6), but not by both simultaneously. Memory addressing consists of both page selection and word selection. A page is defined as 256 bytes; hence, there are four pages per 1K (1024) bytes of memory. Therefore, the CIE Data Memory contains 16 pages on each of the first two boards and 12 pages on the third board. The NCU Data Memory contains only four pages.

Referring to Figure 5-18, sheet 1, Data Memory addressing on a board is accomplished by signal lines MADR05' through MADR16', where MADR05' represents the most significant bit, and MADR16' the least significant bit of the address. For the CIE Data Memory, these 12 lines are bused together for all three boards. Since eight bits are required to select one word of 256, the eight least significant address lines are employed for word selection. A low level on any of these lines represents the active state; hence, highs on MADR16' through MADR09' result in selection of word location zero.

Page addressing on a board is accomplished by the remaining address lines, MADR08' through MADR05'. These four lines allow for selection of 1 of 16 pages. Again, a low on any line is the active condition, and a high on all four lines results in selection of page location zero. MADR05' and MADR06' select the column (1 of 4) of memory chips on a board. When both are low, column 1 is selected; when both are high, column 7 is selected. Selection of a column is accomplished via a low level at the chip select input (pin 13) of the RW04 chips. For the NCU Data Memory, only four pages (column 1 on the board) exist; therefore, MADR05' and MADR06' are always low (connected directly to ground). MADR07' and MADR08' select the page (1 of 4) within a column.

For the CIE Data Memory, page addressing also involves selection of the appropriate one of the three Data Memory Boards. This selection is made via signal line MACS. This line must be set high for the board selected, but low for the other two boards. Hence, a high on this line for board 1 allows access to memory pages 0-15; for board 2, pages 16-31; and for board 3, pages 32-43.

Only one board is involved for the NCU Data Memory. The MACS line of this board is therefore connected directly to V_{cc}.

5.2.5.2 Memory Control (Read/Write)

Referring to Figure 5-18, sheet 1, note that the MACS line going high enables gate C9, pins 1, 2 and 3. This permits a Read/Write control signal to be applied to pin 3 of each RW04 (memory) chip. A high at pin 3 causes the chip to be in the read state; a low at pin 3 causes the chip to be in the write state. The control signal that is routed to pin 3 is fed in via signal lines MOBSBI-1 and MAWRT'-2 which are tied together on the backplane; i.e., backplane terminals 2W and 2V are strapped together. For CIE Data Memory, 2W and 2V of all three boards are strapped together and connected to the write pulse output line from the CIE Ancillary Board.

Writing to memory, then, is accomplished by applying a negative pulse at terminal 2V and 2W. The outputs at pins 6 and 8 of I9, and hence the input at pin 1 of C9, go high. If the input at pin 2 of C9 is high (board selected), the output of C9, pin 3, goes low and applies a write pulse to pin 3 of all RW04 chips. Hence, all those memory locations, whose addresses are active, are written into in accordance with the data applied to the data input pins (pin 11) of the addressed chips (RW04's).

As long as the level at pin 3 of the RW04 chips is high the chips are in the read mode, and data contained in those memory locations whose addresses are active appear at the data output pins (pin 12) of the addressed RW04 chips. The high level from pin 1E is applied to all of the gates of A9 and E9, as shown on Figure 5-18, sheets 4, 5, and 6. Enabling these gates allows data outputs from the selected memory board, via signal lines MPDO10' through MPDO17'.

The required timing relationships between address lines, data input lines, write pulse lines, and data output lines, are listed in Table 5-2 (see paragraph 5.2.4.2).

5.2.5.3 Data Input

Data input is via signal lines MADI10 through MADI17, where MADI10 is the most significant bit and MADI17 is the least significant bit. For the CIE Data Memory, these eight lines are bused together for all three memory boards.

When a data level (high for a logical one, low for a logical zero) appears on any of these lines, and the Read/Write control (pin 3) of the RW04's goes low, the applied data (ones and zeros) is written into the addressed memory location. The required timing relationships of these signals are listed in Table 5-2 (see paragraph 5.2.4.2).

5.2.5.4 Data Output

Data output is via signal lines MPDO10' through MPDO17', where MPDO10' is the most significant bit and MPDO17' is the least significant bit. For the CIE Data Memory, these eight lines are bused together for all three memory boards.

When the Read/Write control level at pin 3 of the RW04's is high, the data contained at the addressed location is fed out via pin 12 of the RW04 chips. Those outputs are gated to the MPDO10' through MPDO17' buses via the application of a high level signal (from pin 1E) to the gates of A9 and E9 shown on Figure 5-18, sheets 4, 5, and 6. The required timing relationships for valid output data are listed in Table 5-2 (see paragraph 5.2.4.2).

5.2.6 NCU ANCILLARY BOARD

The NCU Ancillary Board performs a number of functions required for interfacing several other elements of the ESM. Those other elements, and the NCU Ancillary Board's relationship to them, are shown in Figure 5-21. The specific functions performed are:

a. Word addressing of NCU Data Memory as directed by either the NCU B7* or the CIE B7*.

b. Page addressing of NCU Data Memory as directed by either the NCU B7* or the CIE B7*.

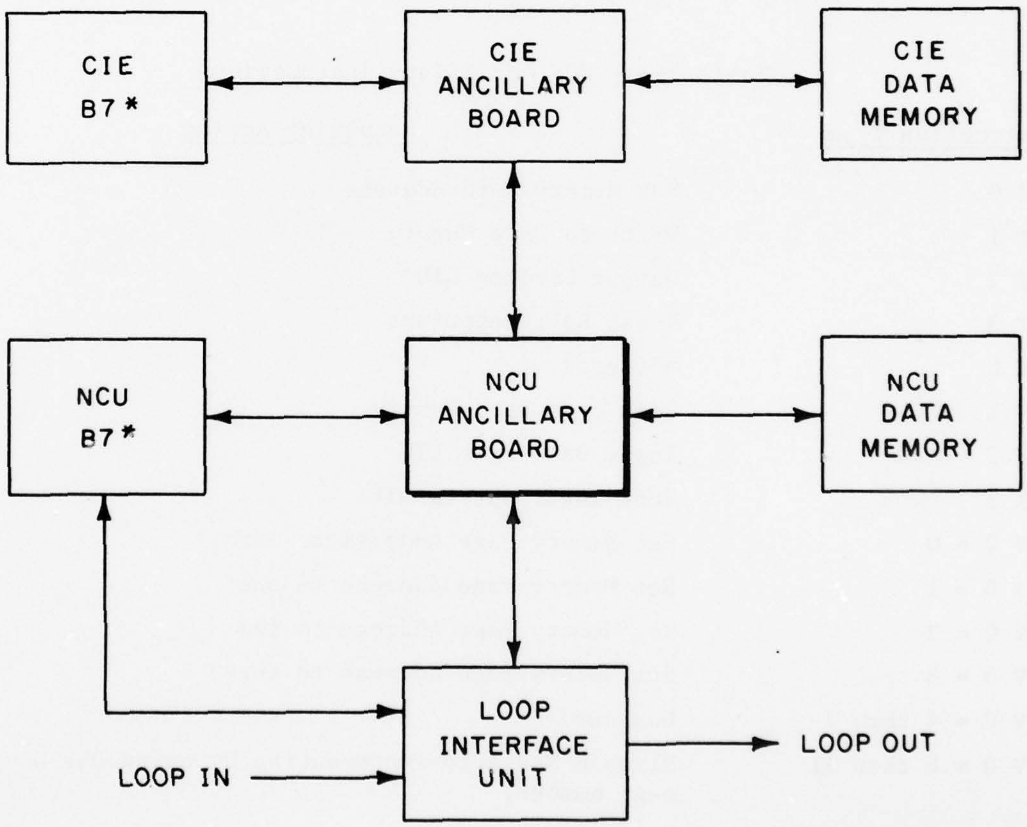


Figure 5-21. NCU Ancillary Board-To-System Interface, Simplified Block Diagram

AD-A063 370 BURROUGHS CORP PAOLI PA FEDERAL AND SPECIAL SYSTEMS GROUP F/G 17/2
EXPLORATORY SYSTEMS CONTROL MODEL (ESM). MAINTENANCE MANUAL.(U)
APR 77 DCA100-75-C-0054

UNCLASSIFIED SBIE-AD-E100 145 NL

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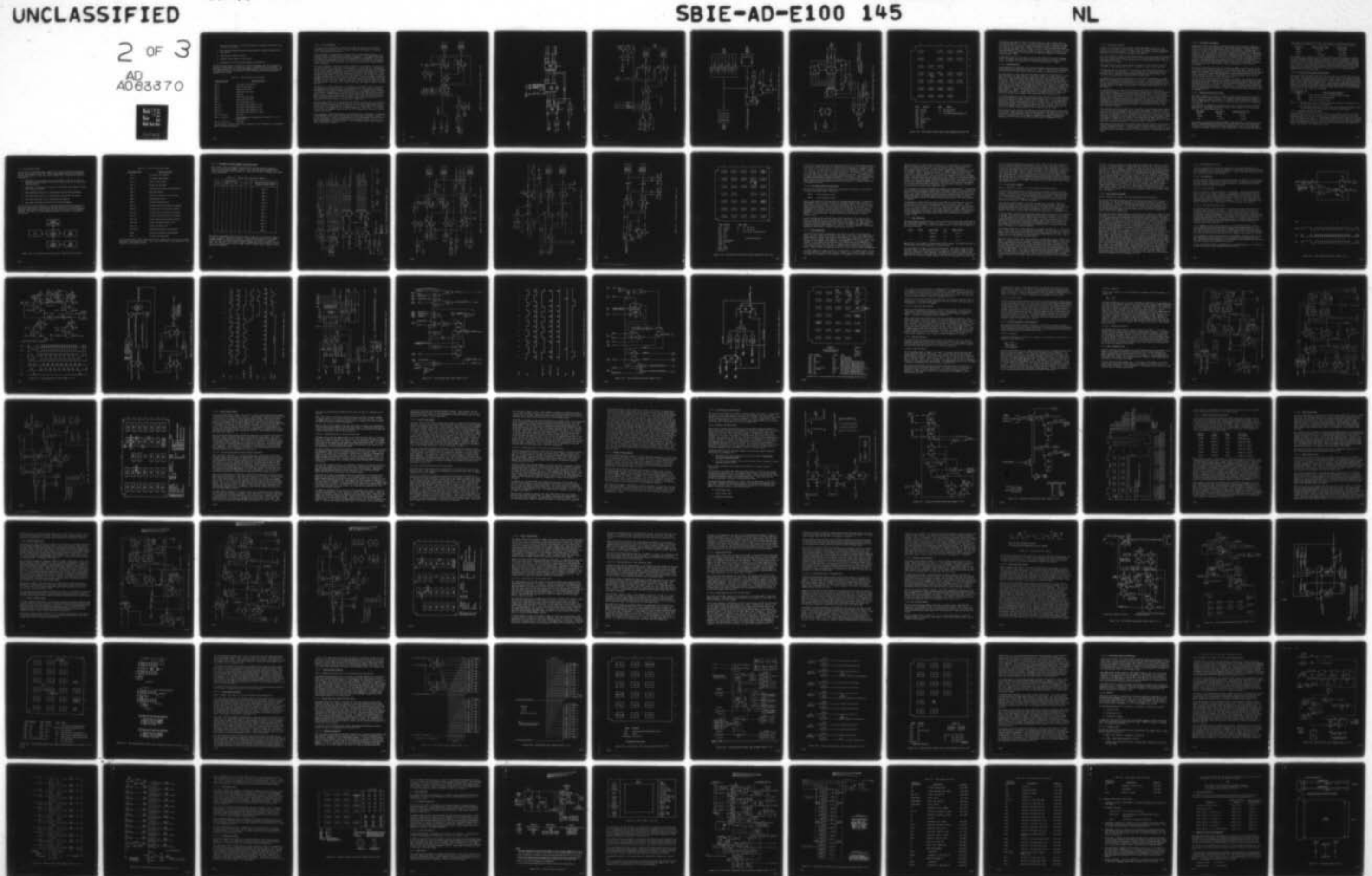
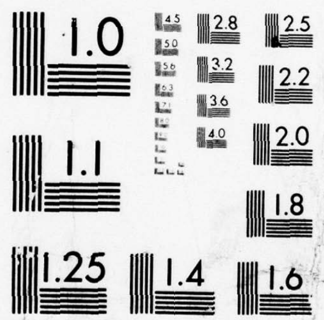




MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

c. Data Input (writing) to the NCU Data Memory from either the NCU B7*, the CIE B7*, or the loop.

d. Data Output (reading) from the NCU Data Memory to either the NCU B7* or the CIE B7*.

e. Generation of time-out clocks.

f. Control of data inputs to the CIE B7*.

g. Generation of a soft interrupt signal to the CIE B7*.

The NCU Ancillary Board's operation is primarily dependent upon the execution of particular instructions, or instruction types, by the NCU B7* or the CIE B7*. The pertinent instructions and actions resulting therefrom are tabulated in Table 5-3 for reference purposes. The details of these resulting actions are presented in paragraphs that follow.

Table 5-3. NCU Ancilliary Instructions

Instruction Type	Resulting Action
OUT 0	Set Memory Word Address
OUT 1	Write to Data Memory
OUT 2	Output Data to LIU
OUT 3	Reset Soft Interrupt
BEX 0	Not used
BEX 1	Read from Data Memory
BEX 2	Input Data from LIU
BEX 3	Soft Interrupt to CIE
DEV 0 = 0	Set Memory Page Address to zero
DEV 0 = 1	Set Memory Page Address to one
DEV 0 = 2	Set Memory Page Address to two
DEV 0 = 3	Set Memory Page Address to three
DEV 0 = 4 thru 7	Not used
DEV 0 = 8 thru 11	Disable MAR Auto-incrementing by using DEV 0 = (8 + page number)
DEV 0 = 12 thru 15	Not used

For each DEV 0 = Literal, that Literal remains set until replaced by a succeeding DEV 0 = Literal Instruction.

5.2.6.1 Word Addressing

Data memory for the NCU B7* is addressed by either the NCU B7* or the CIE B7* in terms of both pages and words. In total, there are four pages of 256 words each. (See Figures 5-22 and 5-23.)

Word addressing is accomplished by an 8-bit counter (Word Address Register) consisting of WAR-1 and WAR-2, shown on Figure 5-22, sheet 1. The eight output lines of this counter are connected to address lines MADR09' through MADR16' of the NCU Data Memory (see paragraph 5.2.5.1). The contents of the counter are initialized to any address and then incremented one count at a time until the largest address (255) is reached.

An initial address is loaded from either the NCU B7*, via an OUT 0 = B instruction, or from the CIE B7*, via an OUT 0 = B instruction. From the NCU B7*, the address enters the NCU Ancillary Board at 1G, is inverted and routed through a switch (WARS) to the input of WADD, an eight-bit serial-in, parallel-out shift register. The address is clocked into WADD by CP0' when enabled by OUT0'. The clock is also routed to WADD by switch WARS. This switch allows the data and clock to WADD to be alternatively selected from the CIE. That is, when DEV 1 = 64, as received at Front Plane terminal 3U from the CIE, is applied to the select input (pin 1) of WARS, the input to WADD is from the CIE B7*. Data and clock enter the NCU Ancillary Board at 3N and 3P, respectively. When DEV 1 = 64 is high (inactive), the input to WADD is from the NCU B7*.

At the end of an OUT 0 instruction, as executed by either NCU or CIE, a load pulse is generated and applied to pin 11 of both WAR-1 and 2. This load pulse strobes the address at the outputs of WADD into WAR-1 and 2. For loading from the NCU B7*, the load pulse is generated by the negative portion of the PRESB' signal as applied to F9, pin 8. A PRESB' signal occurs for every instruction. However, during the OUT 0 instruction, the signal clocks the OUT 0' level (low) into the ARL flip-flop. This low enables NOR gate F9 so that the PRESB' signal occurring during the next instruction cycle will result in a load pulse to WAR-1 and 2.

When an address word is to be loaded from the CIE B7*, the load pulse is received on the NCU Ancillary Board at Front Plane pin 3M, routed through switch WARS, and applied, via pin 11 of NOR gate F9, to WAR-1 and 2. Of course, WARS must be properly set by DEV 1 = 64 (applied to pin 1 of WARS) going low. When DEV 1 = 64' is high, a low on pin 14 of WARS is routed to pin 11 of F9, enabling that NOR gate to permit loading from the NCU.

After loading an initial word address, the address can be incremented. Incrementing is accomplished from the NCU B7* by gating the rising edge of the PRESB' signal to the clock input of WAR-2. Incrementing may also be accomplished from the CIE B7* by the application of the MARI signal to the clock input of WAR-2. The state of WARS, as determined by the level of DEV 1 = 64, establishes which signal is applied to the clock input of WAR-2.

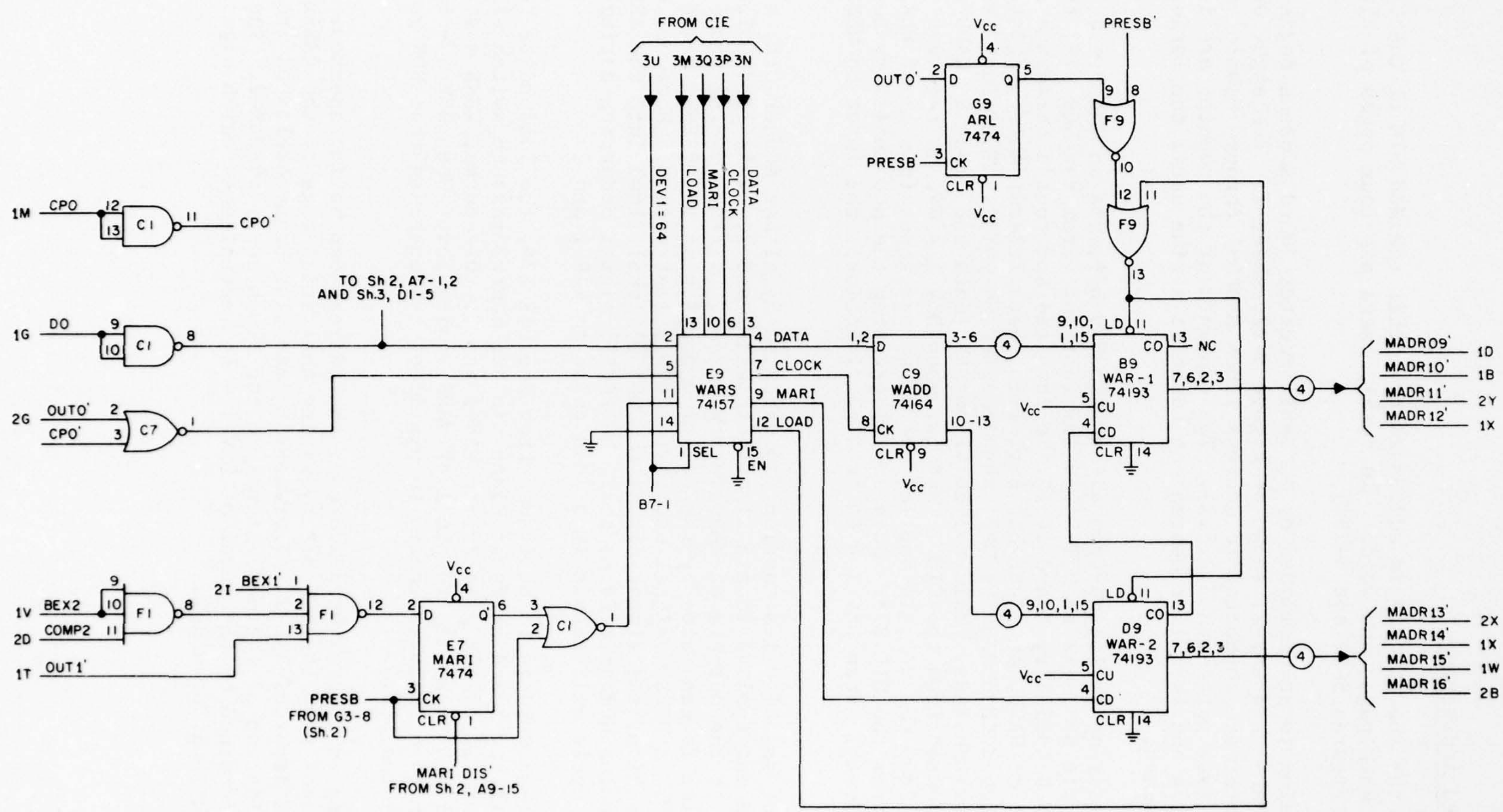


Figure 5-22. NCU Ancillary Board Logic (Sheet 1 of 5)

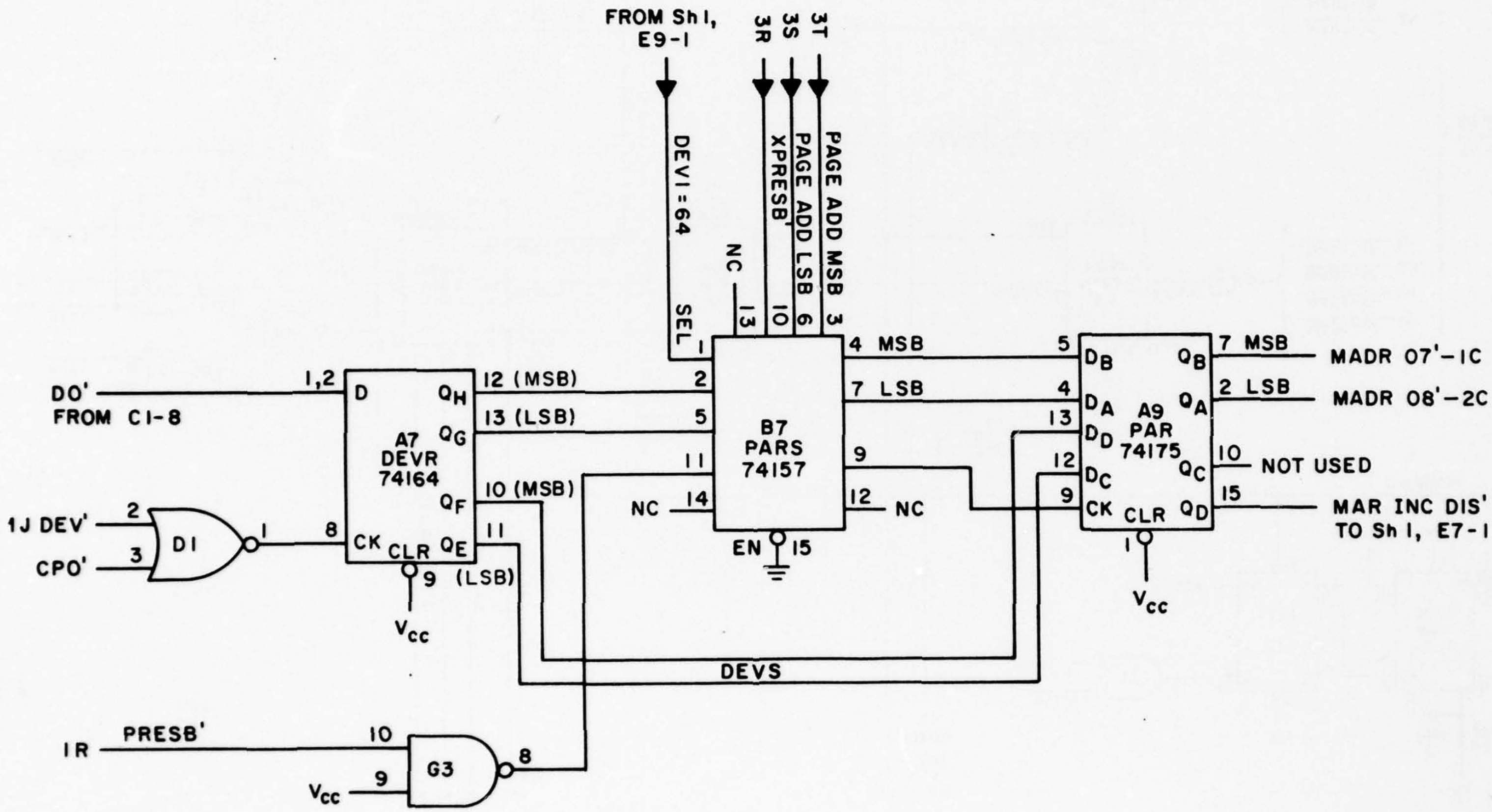


Figure 5-22. NCU Ancillary Board Logic (Sheet 2 of 5)

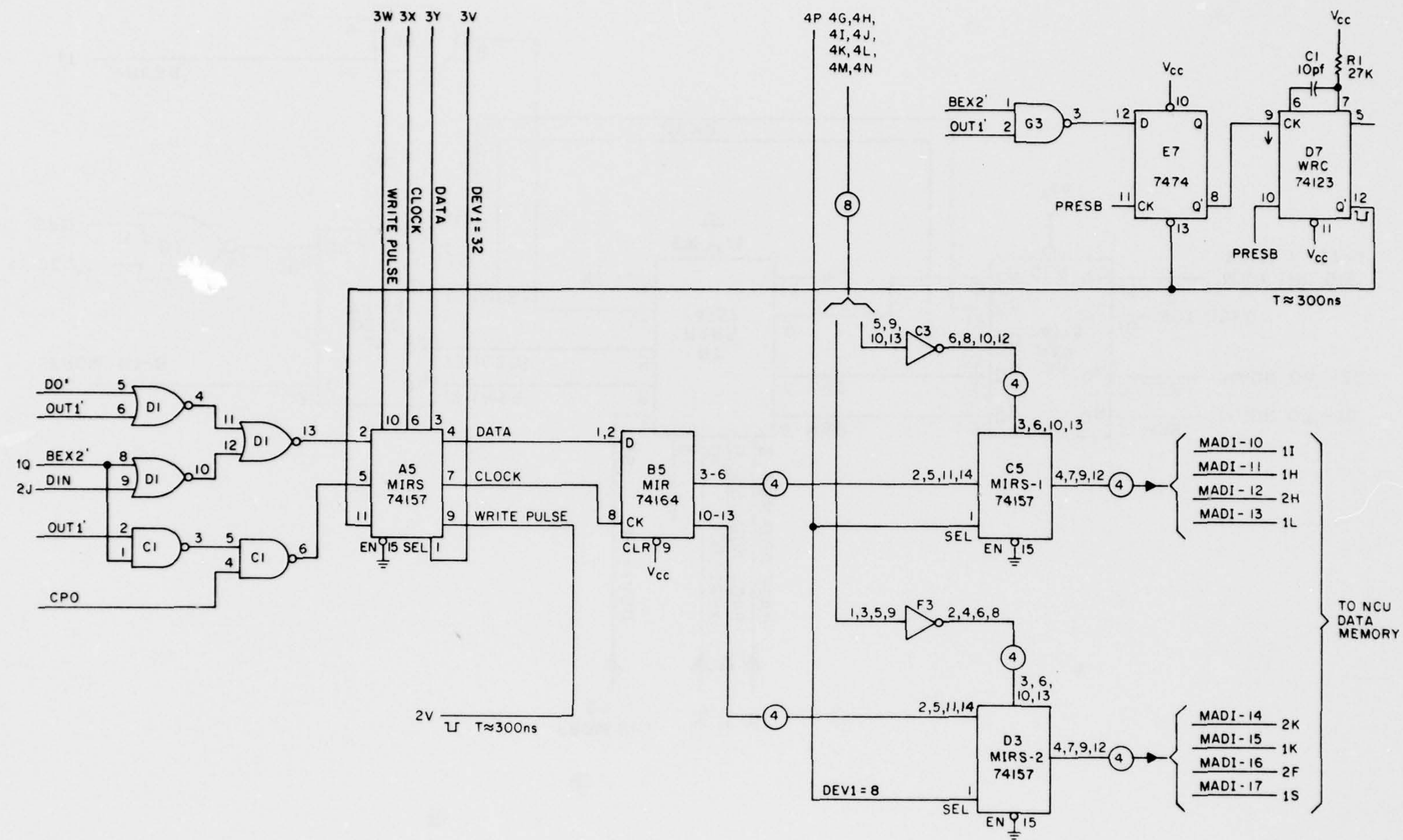


Figure 5-22. NCU Ancillary Board Logic (Sheet 3 of 5)

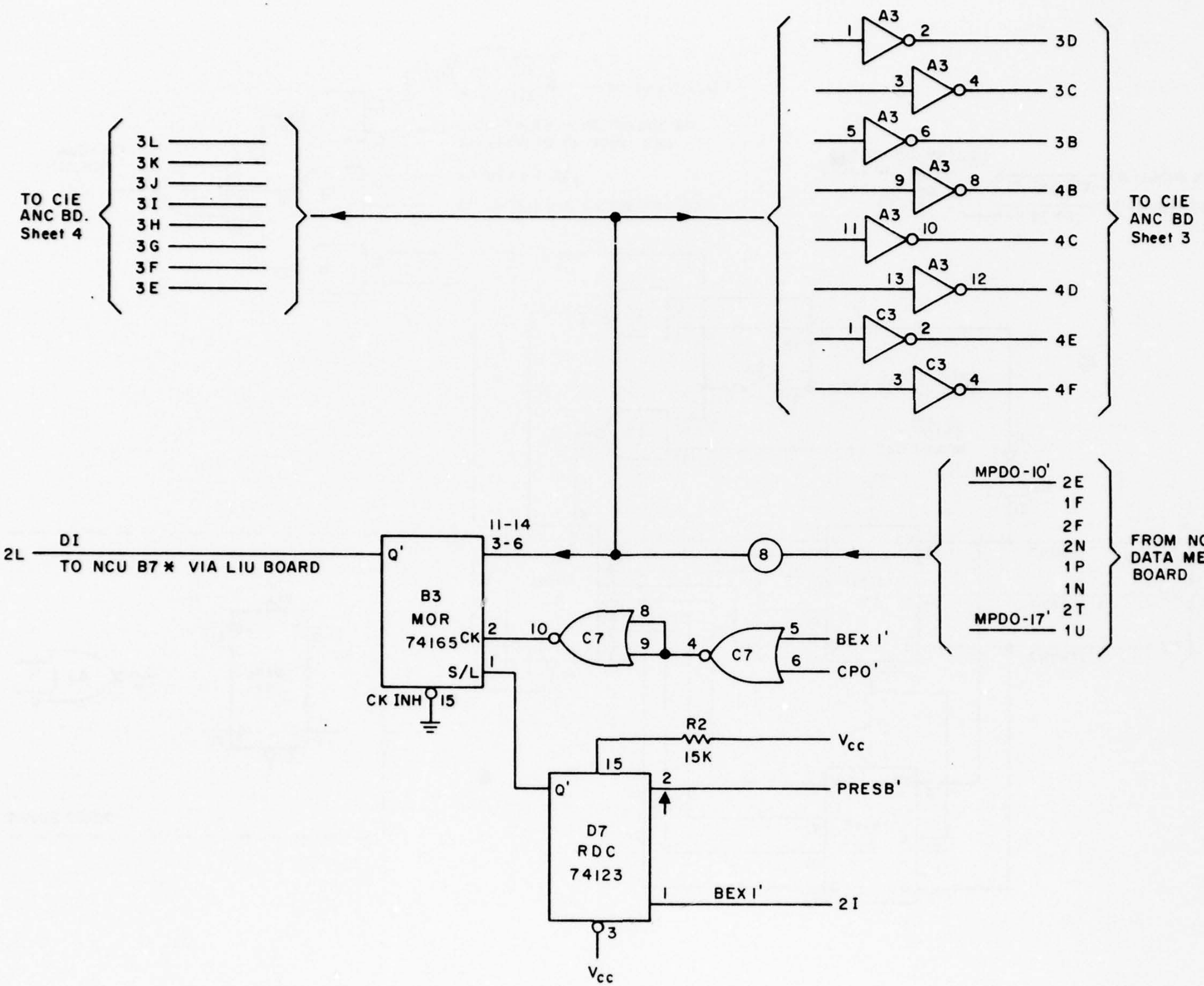


Figure 5-22. NCU Ancillary Board Logic (Sheet 4 of 5)

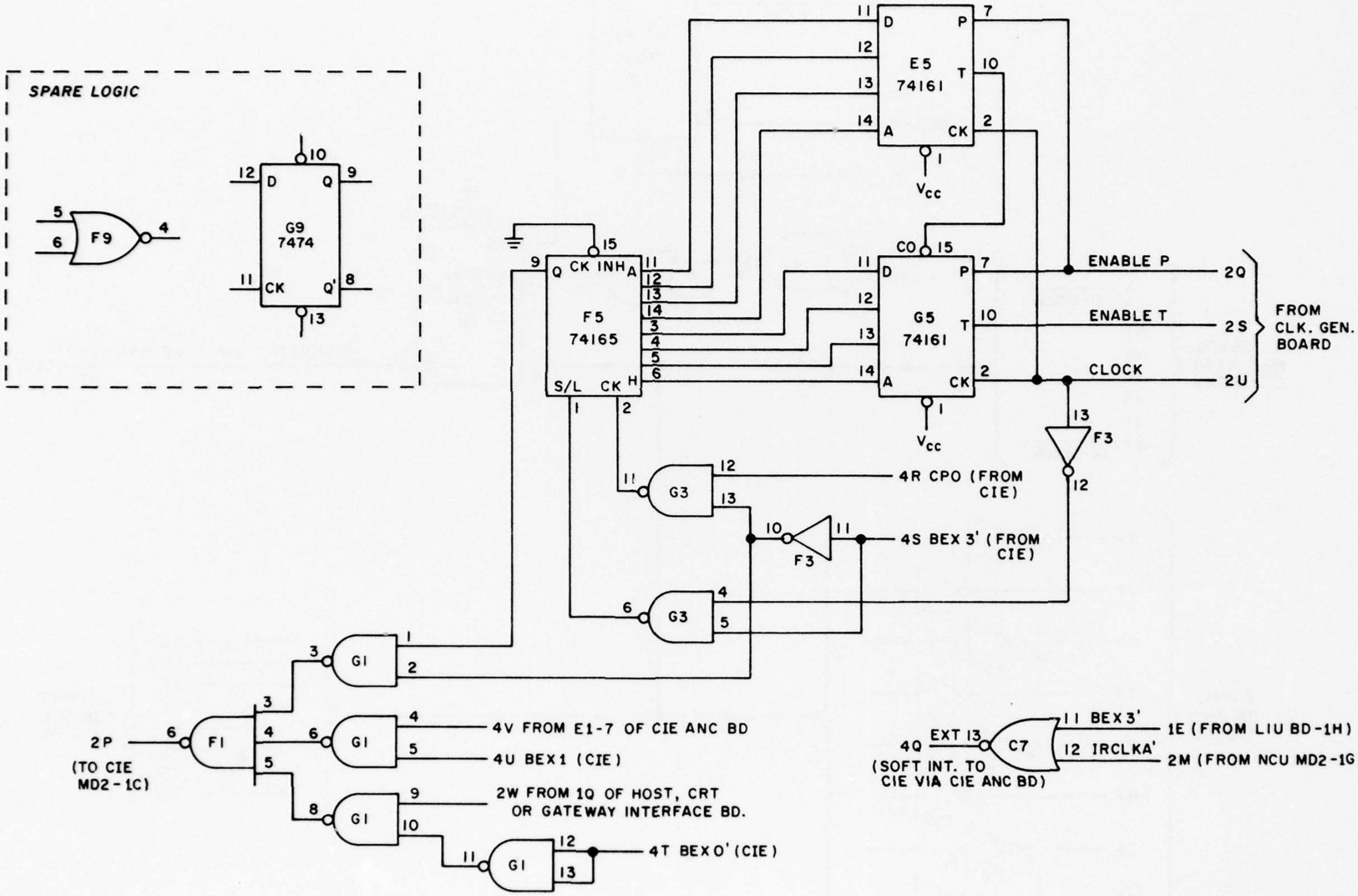
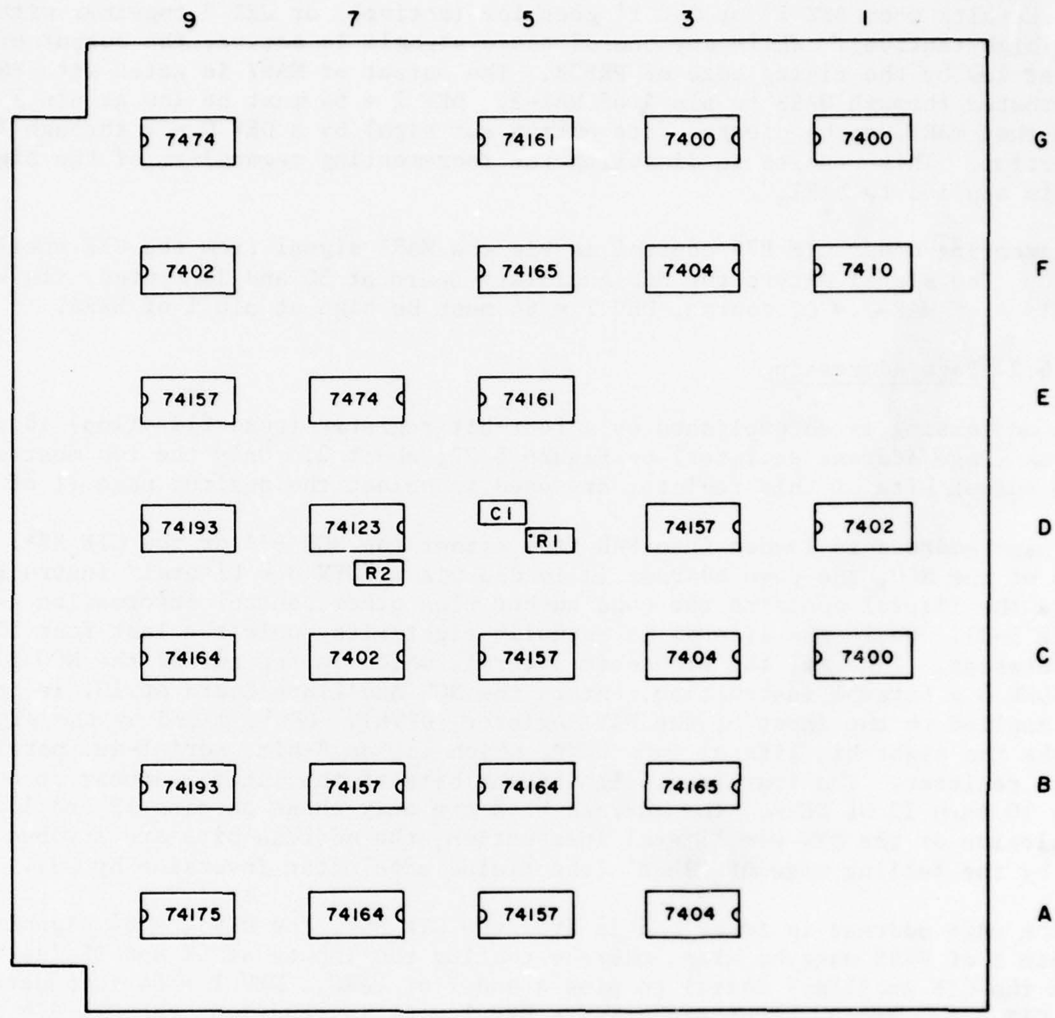


Figure 5-22. NCU Ancillary Board Logic (Sheet 5 of 5)



IDENT	LOCATION
7400	C1, G1, G3
7402	C7, D1, F9
7404	A3, C3, F3
7410	F1
7474	E7, G9
74123	D7
74157	A5, B7, C5, D3, E9
74161	E5, G5
74164	A7, B5, C9
74165	B3, F5
74175	A9
74193	B9, D9

IDENT	VALUE
R1	27K, 1/8W, 5% TOL
R2	15K, 1/8W, 5% TOL
C1	10 PF, 10% TOL, CENTRALAB # DD-100

Figure 5-23. NCU Ancillary Board, Parts Layout Diagram and Parts List

Incrementing under NCU B7* control is enabled when the output of MARI goes low. This results when BEX 1' or OUT 1' goes low (active), or BEX 2 together with COMP 2 goes high (active). While any one of these signals is active, the output of MARI is set low by the rising edge of PRESB. The output of MARI is gated with PRESB and routed through WARS to pin 4 of WAR-2. DEV 1 = 64 must be low at pin 1 of WARS. Note that MARI can be cleared (its output set high) by a DEV 0 = 8 through 11 instruction. This results in disabling the incrementing regardless of the signals levels applied to MARI.

Incrementing under CIE B7* control is via the MARI signal from the CIE Ancillary Board. The signal enters the NCU Ancillary Board at 3Q and is routed, via WARS, to pin 4 of WAR-2. Of course, DEV 1 = 64 must be high at pin 1 of WARS.

5.2.6.2 Page Addressing

Page addressing is accomplished by a four-bit register (quad flip-flop) identified as PAR (Page Address Register) on Figure 5-22, sheet 2. Only the two most significant output bits of this register are used to select the desired page (1 of 4).

The page address is loaded into PAR from either the NCU B7* or the CIE B7*. In the case of the NCU, the page address is loaded via a "DEV 0 = Literal" instruction, where the literal contains the page number plus other control information (see Table 5-3). While the literal is actually eight bits, only the last four bits are of interest. That is, the eight-bit literal, which is fed out of the NCU B7* by the DEV 0 = Literal instruction, enters the NCU Ancillary Board at 1G, is inverted, and applied to the input of the DEV Register (DEVR). CPO', gated by the signal DEV', clocks the eight-bit literal into DEVR, which is an 8-bit, serial-in, parallel-out shift register. The four least significant bits of the literal appear on output pins 10 thru 13 of DEVR. The address bits are only those on pins 12 and 13. After completion of the DEV 0 = literal instruction, the address bits are strobed into PAR by the falling edge of PRESB' (the rising edge after inversion by G3).

If the page address is to be fed in from the CIE NCU, the DEV 1 = 64 signal applied to pin 1 of PARS must be high, thereby routing the inputs at 3T and 3S (as received from the CIE Ancillary Board) to pins 4 and 7 of PARS. DEV 1 = 64 is generated by the CIE B7*. Hence, after executing a DEV 1 = 64 instruction, the CIE B7* can address the NCU memory. The CIE B7* must change the DEV 1 = 64 line back to a low level before the NCU B7* can regain access to its own data memory. Under CIE B7* control, the XPRESB' signal entering at 3R is routed to pin 9 of PAR.

The outputs from pins 10 and 11 of DEVR are routed around PARS and are applied directly to PAR. These inputs are also clocked into PAR by the signal at pin 9 of PAR. They appear at PAR output pins 10 and 15, respectively. Only the output on pin 15 is used. This output is used to enable or disable the automatic incrementing capability of WAR-1 and 2 as controlled by MARI (refer to paragraph 5.2.6.1).

5.2.6.3 Data Input to Memory

The NCU Ancillary Board accepts eight-bit data words (bytes) from one of four sources: (1) the NCU B7*, (2) the loop, via the LIU board, (3) the CIE Ancillary Board, and (4) CIE Data Memory. It routes these data words to NCU Data Memory as described below, and illustrated in Figure 5-22, sheet 3.

Data from the NCU B7* enters the NCU Ancillary Board at 1G (see Figure 5-22, sheet 1) and, after inversion, appears at D1, pin 5. It is clocked into MIR (via MIRS) by CPO, when gated by OUT 1'. Note that when OUT 1' is low (active), BEX 2' must be high; hence, C1-3 is high.

Data from the loop enters the NCU Ancillary board at 2J and is clocked into MIR (via MIRS) by CPO, when gated by BEX 2'. When BEX 2' is low, OUT 1' is high.

In order for data from the NCU B7* or the loop to enter MIR, the SEL signal at pin 1 of MIRS must be low (inactive). If SEL is high, data to MIR is from the CIE Ancillary Board. This data and associated clock enter the NCU Ancillary Board at 3Y and 3X, respectively, and are routed via MIRS to MIR.

As indicated, data to MIR is the result of: (1) An OUT 1 instruction, or a BEX 2 instruction as executed by the NCU B7*, or (2) an OUT 2 instruction preceded by a DEV 1 = 32 instruction, both executed by the CIE B7*. At the conclusion of each of these instructions, the 8-bit data byte is contained in MIR and applied, in bit-parallel fashion, via MIRS-1 and 2, directly to the data input lines of the NCU Data Memory.

As indicated above, the data from the CIE Data Memory may be routed directly to the NCU Data Memory. This is accomplished in bit-parallel via the NCU Ancillary Board inputs 4G through 4N, and via the switches MIRS-1 and 2. For this operation, a DEV 1 = 104 instruction must be executed by the CIE B7*. This instruction results in the signals DEV 1 = 64, DEV 1 = 32, and DEV 1 = 8 being active until the next DEV 1 = Literal instruction is executed by the CIE B7*. A data word is transferred in parallel from the CIE Data Memory to the NCU Data Memory for each CIE instruction cycle time for which the DEV 1 = 104 condition is set. Hence, after 256 cycle times, a complete data packet (256 words) will have been transferred (memory-to-memory).

While the data outputs from MIRS-1 and 2 are applied to the NCU Data Memory inputs, a write pulse must be applied to memory control input MAWRT'. This write pulse is generated by the one shot WRC if the data input was from the NCU B7* or the loop; that is, if an NCU OUT 1 or BEX 2 instruction were the cause of the data. In these cases WRC is triggered by the falling edge of the output of E7, while PRESB is high. The output of E7 goes low as a result of the rising edge of PRESB, provided that either BEX 2' or OUT 1' is low (active). The output of WRC, which must be at least 250 nsces (preferably 300 nsecs), is routed, via MIRS, to pin 2V.

When data is fed in from the CIE Ancillary Board, the write pulse is also received from the CIE Ancillary Board. It enters the NCU Ancillary Board at 3W and is routed, via MIRS, to pin 2V. In this case DEV 1 = 32 must be high at pin 1 of MIRS. The write pulse, when received from the CIE Ancillary Board, is approximately 430 nsecs.

5.2.6.4 Data Output from Memory

Referring to Figure 5-22, sheet 4, the NCU Ancillary board accepts an eight-bit parallel data word (byte) from NCU Data Memory and routes it to either the NCU B7*, via 2L, or to the CIE Ancillary Board, via two sets of lines. The data word is routed to the NCU B7*, via MOR, in response to the NCU B7* executing the BEX 1 instruction. That is, when BEX 1' at pin 1 of RDC goes low (active) it is immediately followed by the rising edge of PRESB' which triggers the one shot, RDC. The output of RDC loads the signals at pin 11-14 and 3-6 of MOR into MOR. The eight clock pulses of CPO' gated by BEX 1' (at pins 6 and 5 of C7), clock this data out of MOR. This data exits the NCU Ancillary Board at 2L and is routed to the NCU B7*'s B-Register. The NCU can then further manipulate this data, or can output it directly to the loop via an OUT 2 instruction. Refer to paragraph 5.2.8 for the LIU description.

The eight-bit parallel data words from the NCU Data Memory are also always present on the two sets of lines that connect to the CIE Ancillary Board. The set on the upper left of Figure 5-22, sheet 4, are routed to the input of the CIE B7* and thereby permit the CIE B7* to access NCU Data Memory. This is accomplished by the CIE B7* via its execution of DEV 1 = 96 and BEX 1, A1 = A1 instructions. Refer to CIE Ancillary Board description given in paragraph 5.2.7.

The set of lines at the upper right of Figure 5-22, sheet 4, are routed to the input data lines of the CIE Data Memory and allow direct memory-to-memory transfers under command of the CIE B7*. That is, the CIE sets initial addresses for both memories, then executes the DEV 1 = 80 (DEV 1 = 64 and DEV 1 = 16 signals active) instruction. After 256 CIE instruction times, a complete packet of 256 bytes will have been transferred from NCU Memory-to-CIE Memory. Refer to CIE Ancillary Board description given in paragraph 5.2.7.

5.2.6.5 Generation of Time Out Clocks

Referring to Figure 5-22, sheet 5, a time out clock is derived for use by the CIE B7*. This clock is used by the CIE B7* to determine relative time with respect to events relating to time-out actions. For example, a NAK is assumed if neither an ACK nor a NAK has been received during a specified time duration after transmission of a message.

Clock and control signals are accepted at pins 2Q, 2S, and 2U, from the Clock Generator Board. The actual clock rate received at 2U is related to the loop speed selected, e.g., High, Medium, or Low.

Loop Speed	Input at 2U	Effective Clock Rate
High	96 KHz	23.4 Hz
Medium	28 KHz	6.8 Hz
Low	1.2 KHz	0.29 Hz

As a result of the gating provided by ENABLE P (6K pulses/sec at the High rate) and ENABLE T (approximately 23.4 pulses/sec at the High rate), the counter consisting of E5 and G5 has the effective clock rates shown above. That is, the least significant bit changes at that rate. This corresponds to once every 1024 information

characters at the selected loop rate. The counter is continuous in that it recycles after 256 counts; hence, count times and recycle times are as follows:

Loop Rate	Period of Each Count	Recycle Time
High	42.7 ms.	10.9 secs.
Medium	1[illegible]6 ms.	37.4 secs.
Low	3.4 secs.	87.5 secs.

The contents of the counter are read by the CIE B7* via the execution of a BEX 3, A3 = A3 instruction, which results in transfer to the B7*'s B-Register. That is, the BEX 3' signal at 4S when gated with the clock from 2U, provides a load signal (low) at pin 1 of F5 thereby loading the contents of the counter (E5 and G5) into F5. While BEX 3' is still active (low), it gates CP0, via G3, to the clock input (pin 2) of F5, thereby shifting (clocking) the newly loaded contents of F5 to the B-Register of the CIE B7*. Note that the level on pin 1 of F5 must be high to permit F5 to be in the shift mode.

5.2.6.6 Control of Data Inputs to the CIE B7*

The output of F5 (on Figure 5-22, sheet 5) is routed to the CIE B7* MD2 board (pin 1C on MD2). This path is from pin 9 of F5, via pins 1 and 3 of G1, pins 3 and 6 of F1, and out of the NCU Ancillary Board at 2P. Other outputs from the NCU Ancillary Board to the CIE B7* are also gated via 2P. That is, G1-4, 5 and 6; F1-8, 9 and 10; F1-4, 5 and 6 permit other outputs via 2P. However, this gating permits only one output at a time and is dependent upon the specific BEX instruction executed by the CIE B7*. The result is one input to the data input port at pin 1C on the MD2 board of the CIE B7*. The inputs are as follows:

CIE B7* Instructions (Note 1)	Input Permitted (Note 2)
BEX 0	Input from Host, CRT, or Gateway Interface board.
BEX 1	Input from CIE Ancillary Board.
BEX 3	Input from Time-Out Clock.

Notes: 1. Refer to Table 5-4 of CIE Ancillary Board Description (paragraph 5.2.7) for BEX type instruction assignments.

2. For additional description of the above listed "Inputs Permitted", refer to the related board descriptions contained in this manual.

5.2.6.7 Generation of Soft Interrupt

A soft interrupt is generated by the NCU B7*, via execution of a BEX 3 type of instruction, per Table 5-3, and routed to the EXT (interrupt) flip-flop on the CIE Ancillary Board. As a result of the BEX type instruction, BEX 3' goes low at pin 11 of C7 (see Figure 5-22, sheet 5). When IRCLKA' goes low, at pin 12 of C7, an output (high) is available at pin 13 of C7 and is routed from 4Q of the NCU Ancillary Board to 3Q of the CIE Ancillary Board, and on to the EXT flip-flop on that board (see Figure 5-25, sheet 1, and paragraph 5.2.7.2).

5.2.7 CIE ANCILLARY BOARD

The CIE Ancillary Board performs a number of functions required for interfacing several other elements of the ESM. Those other elements, and the CIE Ancillary Board's relationship to them, are shown in Figure 5-24. The specific functions performed are:

a. Decoding of control signals and control words for the CIE in order to generate control signals for use on this board as well as on other interconnected boards.

b. Generation of interrupts for output to the NCU B7*, and receipt of interrupts from the NCU B7*.

c. Word addressing relative to accessing both CIE and NCU data memory.

d. Page addressing relative to accessing both CIE and NCU data memory.

e. Data input (writing) to both CIE and NCU data memory.

f. Data output (reading) from both CIE and NCU data memory.

The CIE Ancillary Board's operation is dependent primarily upon the execution of particular instructions or instruction types by the CIE B7*. The pertinent instructions and the actions which result are tabulated in Table 5-4 for reference purposes. The details of these resulting actions are presented in paragraphs that follow.

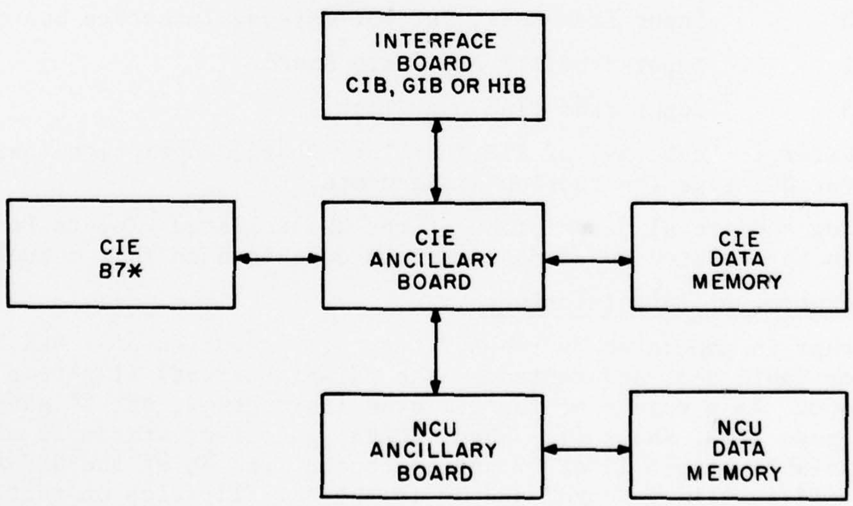


Figure 5-24. CIE Ancillary Board Interfacing, Simplified Block Diagram

Table 5-4. CIE B7* Instruction Types

Instruction Type	Resulting Action
OUT 0	Set Memory Word Address
OUT 1	Set Memory Page Address
OUT 2	Write to Data Memory
OUT 3	Reset Soft Interrupt
BEX 0	Read Interface Buffer Status Register
BEX 1	Read Data Memory
BEX 2	Initialize Interface Data Transfer
BEX 3	Read Time-Out Clock
DEV 0	CIE Soft-Interrupts NCU
DEV 1=1	Terminate NCU-to-CIE Parallel Transfer
DEV 1=2	Initiate IB-to-CIE Parallel Transfer
DEV 1=4	Initiate CIE-to-IB Parallel Transfer
DEV 1=8	Initiate CIE-to-NCU Parallel Transfer
DEV 1=16	Initiate NCU-to-CIE Parallel Transfer
DEV 1=32	Connect NCU MIR and MOR to CIE
DEV 1=64	Connect NCU MAR to CIE
DEV 1=128	Disable MAR Automatic Incrementing
DEV 2	Initialize Interface Data Transfer
DEV 3	CIE Hard Interrupts NCU

The right-hand side of DEV 1 instructions can be combinations of the literals shown above, e.g., DEV 1=80 or DEV 1=94. Also, each literal that is set remains set until replaced by a succeeding literal.

5.2.7.1 Decoding of Control Signals and Control Words

Four control lines are accepted from the CIE B7* and are decoded to generate a total of twelve control signals. These control lines and the resulting control signals are tabulated below in Table 5-5. They are also shown on Figure 5-25, sheet 1, and Figure 5-26.

Table 5-5. Control Lines and Control Signals

Control Lines				Resulting Control Signals (Signal Active=0 State)
SEL A	SEL B	N9	N10	
1	1	0	0	DEV' 0
1	1	0	1	DEV' 1
1	1	1	0	DEV' 2
1	1	1	1	DEV' 3
1	0	0	0	OUT' 0
1	0	0	1	OUT' 1
1	0	1	0	OUT' 2
1	0	1	1	OUT' 3
0	1	0	0	BEX' 0
0	1	0	1	BEX' 1
0	1	1	0	BEX' 2
0	1	1	1	BEX' 3
0	0	X	X	NONE

The control lines SELA, SELB, N10 and N9 enter on pins 1M, 1J, 2D, and 1R, respectively, as shown on Figure 5-25, sheet 1. These lines are decoded by the Control Decoders (CDEC's) to produce active signals having a zero level. It should be noted that only one of the resulting control signals can be active (low) at a given time. The opposite state (active = high) of most of these control signals is also derived via inverters.

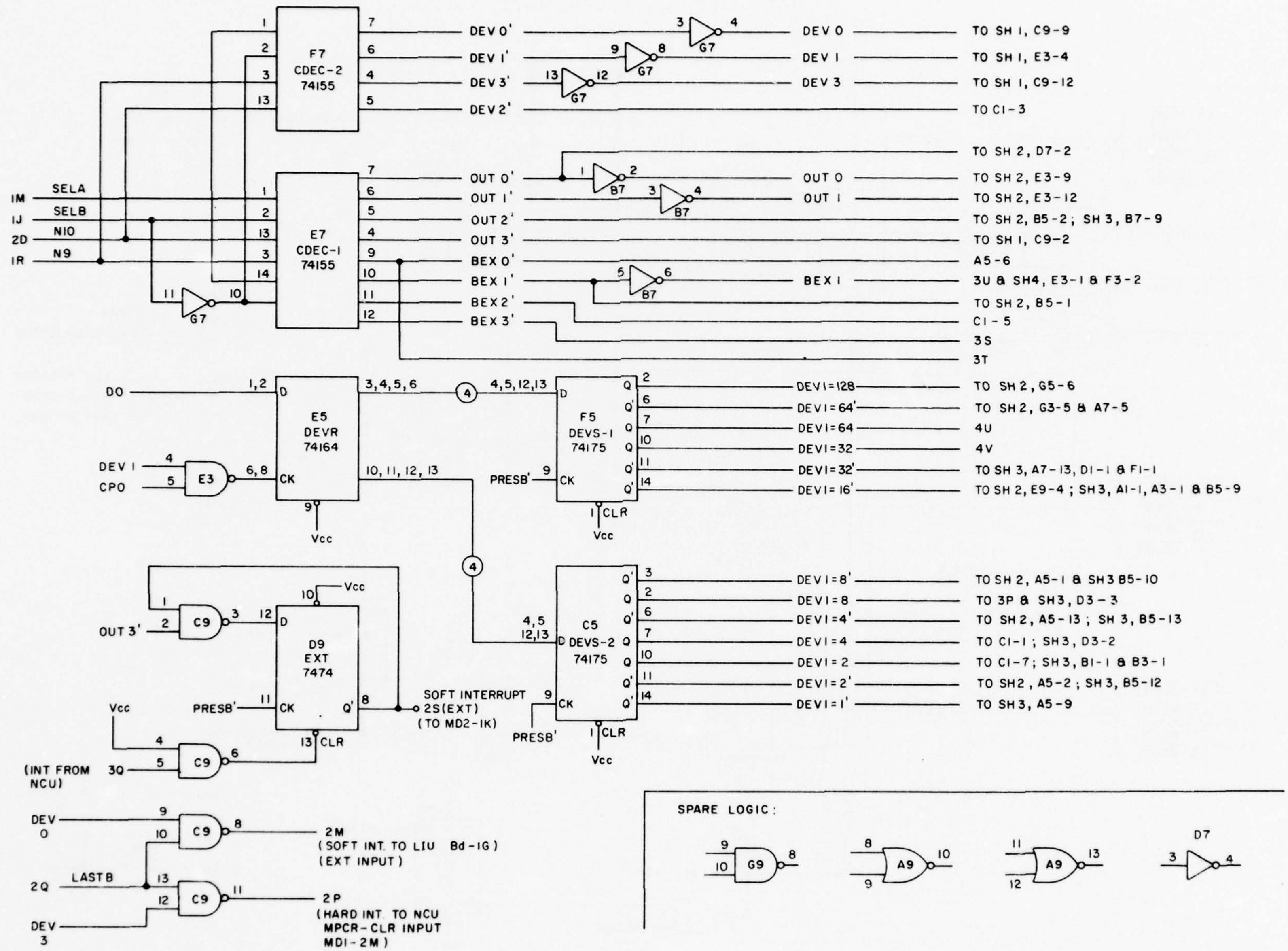


Figure 5-25. CIE Ancillary Board Logic (Sheet 1 of 4)

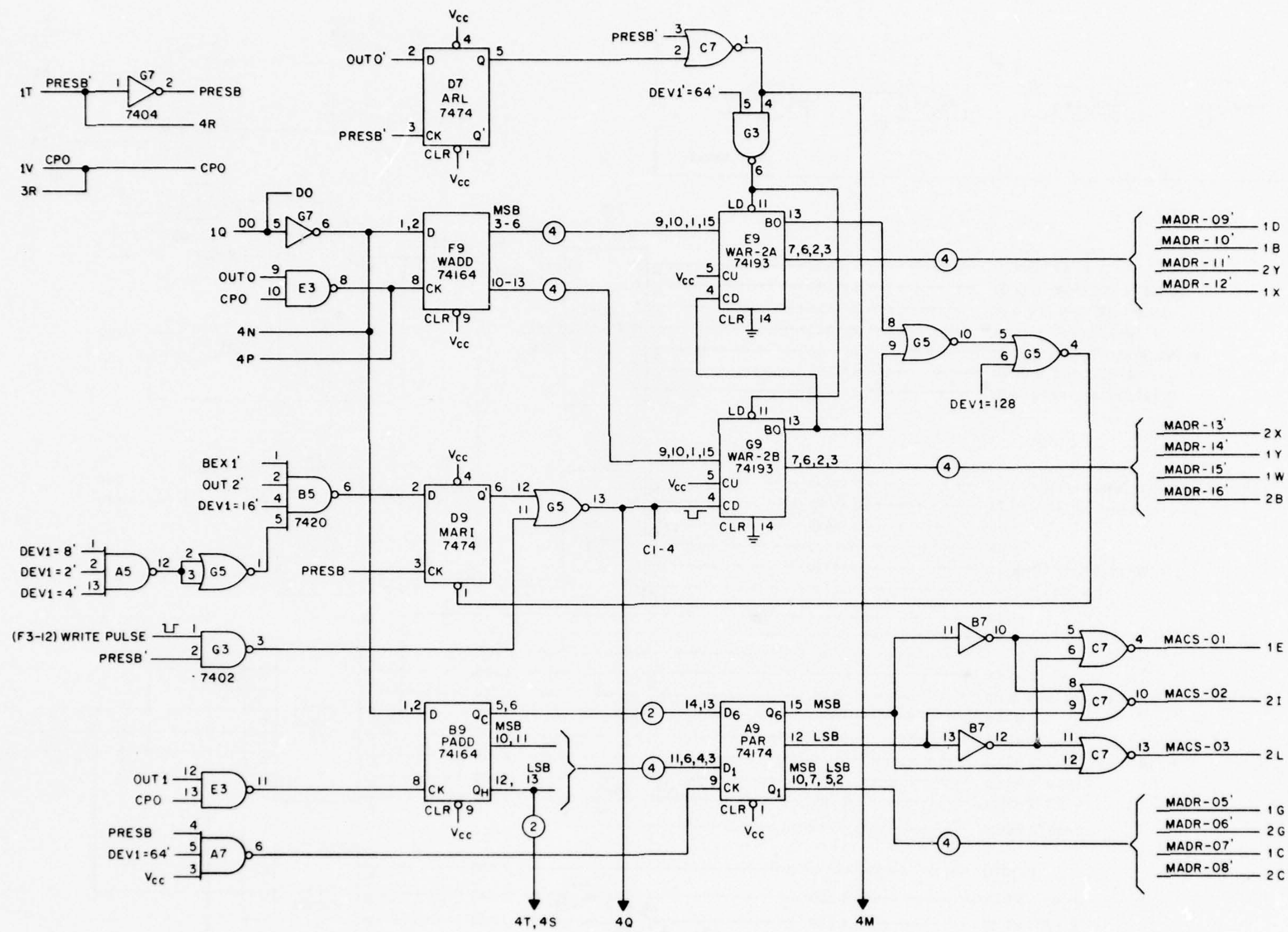


Figure 5-25. CIE Ancillary Board Logic (Sheet 2 of 4)

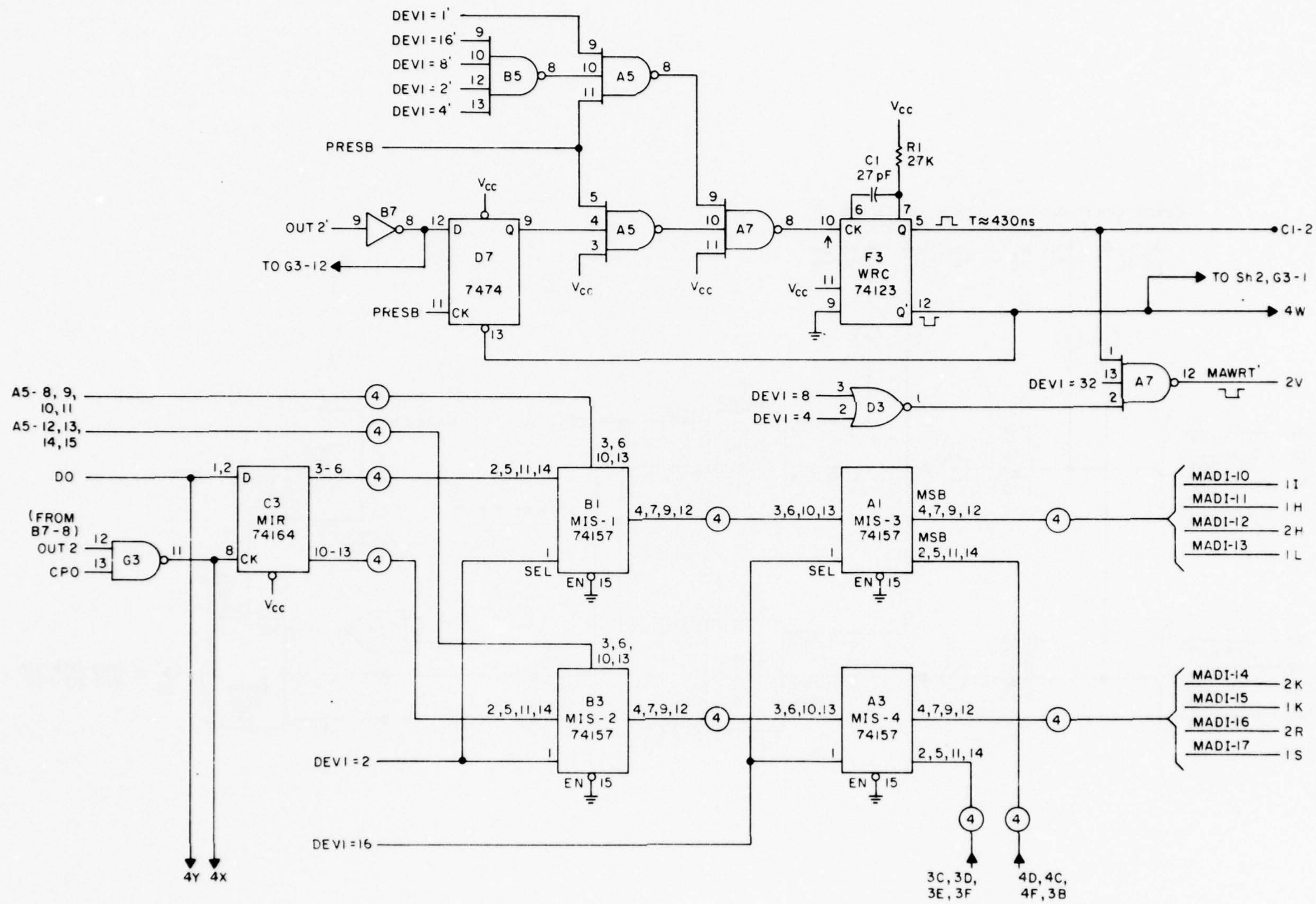


Figure 5-25. CIE Ancillary Board Logic (Sheet 3 of 4)

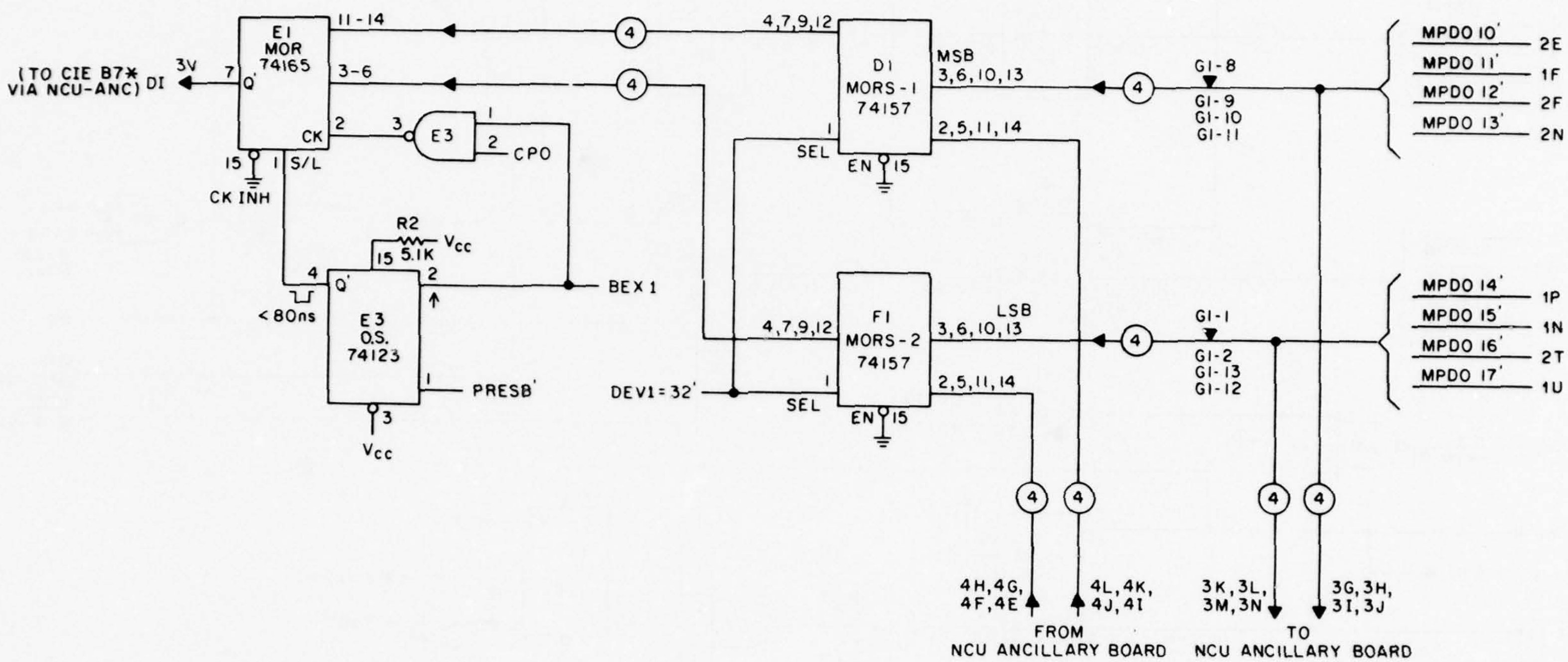
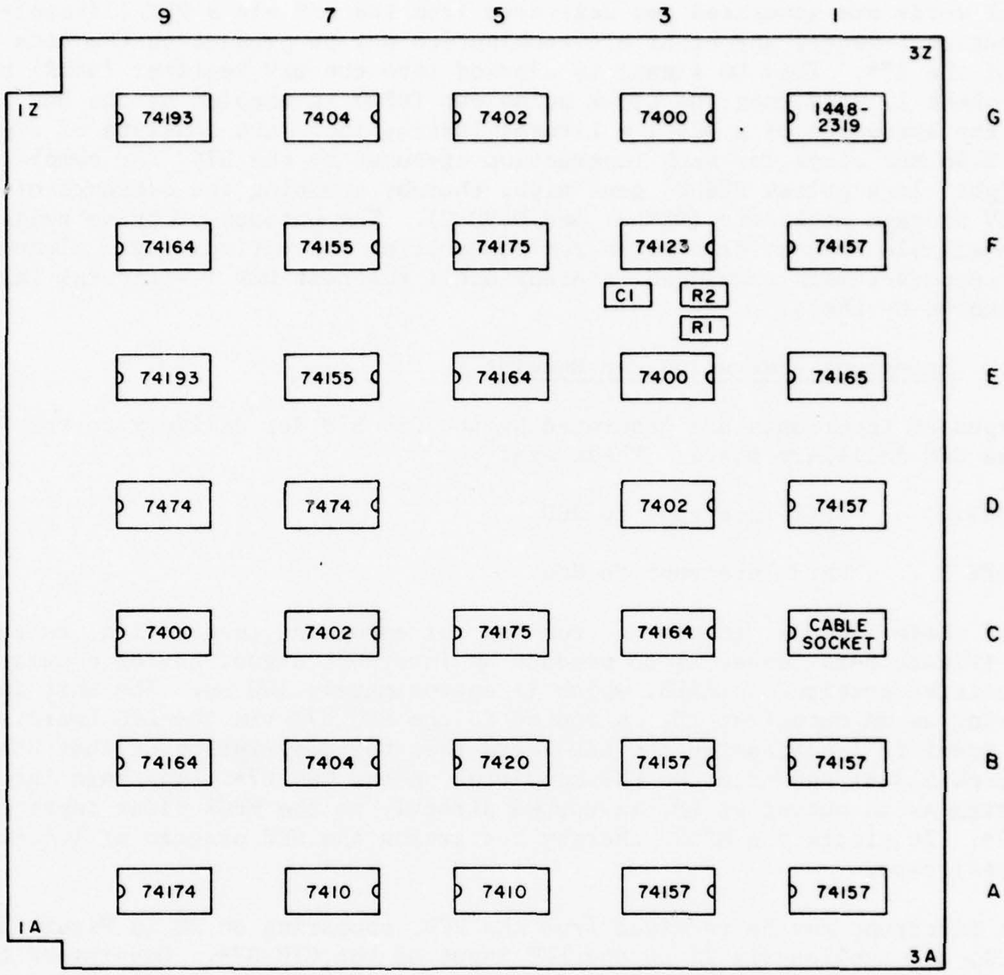


Figure 5-25. CIE Ancillary Board Logic (Sheet 4 of 4)



IDENT	LOCATION
7400	C9, E3, G3
7402	C7, D3, G5
7404	B7, G7
7410	A5, A7
7420	B5
7474	D7, D9
74123	F3
74155	E7, F7
74157	A1, A3, B1, B3, D1, F1
74164	B9, C3, E5, F9
74165	E1
74174	A9
74175	C5, F5
74193	E9, G9
*1448-2319	G1

IDENT	VALUE
R1	27K, 1/8W, 5% TOL.
R2	5.1K, 1/8W, 2% TOL.
C1	27 Pf, 10% TOL., CENTRALAB # DD-270

* BURROUGHS RESISTOR DIP

Figure 5-26. CIE Ancillary Board, Parts Layout Diagram and Parts List

Control words are generated and delivered from the B7* via a DEV (literal-to-device) instruction. Hence, any eight bit combination may be present on the Data Out (DO) line of the B7*. This DO signal is clocked into the DEV Register (DEVR) of Figure 5-25, sheet 1, only when the clock pulse out (CPO) is enabled by the DEV 1 signal, i.e., the execution of a DEV 1 = Literal Instruction. CPO consists of eight pulses of an 8.96 MHz clock for each instruction executed by the B7*. At completion of the eight clock pulses PRESB' goes high, thereby strobing the contents of DEVR into the DEV Storage Registers (DEVS-1 and DEVS-2). The outputs of these registers are then available as control signals for controlling the various logic elements. These outputs remain unchanged (stored) until the next DEV 1 = Literal instruction is executed by the B7*.

5.2.7.2 Interrupt Generation and Receipt

Two types of interrupts are generated by the CIE B7* for delivery to the NCU B7* via the CIE Ancillary Board. These are:

DEV 0	Soft Interrupt to NCU
DEV 3	Hard Interrupt to NCU

Each of these signals, resulting from the corresponding instruction, is gated with LASTB (Figure 5-25, sheet 1) to produce an interrupt signal having a duration of the positive portion of LASTB, which is approximately 100 ns. The soft interrupt, appearing as an output at 2M, is routed to the NCU B7* via the LIU board. It performs specific functions on the LIU board (see the description of that board in paragraph 5.2.8) and sets the EXT condition on the NCU B7*. The hard interrupt, appearing as an output at 2P, is routed directly to the MPCR clear input of the NCU B7*. It clears the MPCR thereby restarting the NCU program at location (address) zero.

A soft interrupt may be received from the NCU, appearing on 3Q in Figure 5-25, sheet 1, and applied via 2S to the EXT input of the CIE B7*. Receipt of the soft interrupt clears the EXT Flip-Flop, setting the level high at 2S. This high level holds the flip-flop cleared until OUT 3' goes low and PRESB' goes high thereby setting the flip-flop and allowing 2S to go low. In effect, the OUT 3 instruction, executed by the CIE B7*, is used to reset the EXT condition.

5.2.7.3 Word Addressing

Data memory for the CIE is addressed by the CIE B7* in terms of both pages and words. In total, there are 44 pages of 256 words, 8 bits each. Word addressing is accomplished by an 8-bit counter (Word Address Register) consisting of WAR-2A and WAR-2B. Refer to Figure 5-25, sheet 2. The eight output lines of this counter are connected to the address lines (MADR-09' through MADR-16') of the data memory. The contents of the counter are initialized to any address and then decremented one count at a time until the count zero is reached, which corresponds to address 255 at the memory location (as a result of inverters on the inputs of the Data Memory Board). Memory address incrementing occurs as a result of this counter decrementing.

An initial address is loaded via OUT 0 = B instruction. The address enters the CIE Ancillary Board at 1Q and, after inversion, appears at the input to WADD, an eight bit serial-in, parallel-out, shift register. The address is also routed to the NCU

Ancillary Board via a Front Plane connection at 4N. The address is clocked into WADD by CPO when enabled by OUT 0. At the end of the OUT 0 instruction a load pulse is generated and applied to WAR2A and WAR-2B, thereby transferring the address to WAR-2A and 2B. The load pulse is generated by the negative portion of the PRESB' signal as applied at C7, pin 3. A PRESB' signal occurs for every instruction. However, during an OUT 0 instruction, it clocks the OUT 0' level (low) into the ARL Flip-Flop. This low enables the NOR gate C7 so that the PRESB' signal, occurring during the next instruction, will result in a load pulse to WAR-2A and 2B. DEV 1=64' must be high during the time that an OUT 0 =B is executed for the purpose of loading word address into the CIE Ancillary Board. When DEV 1 = 64' is low (active), loading of WAR-2A and 2B is inhibited, but loading of a word address into the NCU Ancillary Board is permitted. The load pulse is routed to the NCU Ancillary Board via Front Plane connection at 4M.

After loading an initial word address, the address can be incremented. Incrementing is accomplished by gating the rising edge of the PRESB' signal to the clock input of WAR-2B. This same increment signal is also routed to the NCU Ancillary Board, via Front Plane connection 4Q, and to External Device Interface Board, via C1-4 and the inter-board cable. The PRESB' signal is gated with the write pulse to prohibit address incrementing until the write pulse goes high; that is, the write operation is complete.

Incrementing is enabled when the output of the MARI flip-flop goes low. This low results when any one of the following signals go low (active): BEX 1', OUT 2', DEV 1=16', DEV 1=8', DEV 1=2', or DEV 1=4'. While any one or more of these signals is low, the output of MARI is set low by the rising edge of PRESB. MARI can be cleared (its output set high) by a DEV 1=128 instruction, thereby prohibiting incrementing regardless of the levels of the other signals listed above. Incrementing is also disabled when the Borrow Outputs (BO's) of both WAR-2A and 2B are low (address = 255).

5.2.7.4 Page Addressing

Page addressing is accomplished by a six-bit register (hex flip-flop), identified as PAR (Page Address Register) on Figure 25, sheet 2. The two most significant bits of PAR are used to select one of three data memory boards. A high level is applied to the boards selected.

A9-15	A9-12	Signal Name	Pin	Memory Board
1	1	MACS-01	1E	No. 1
1	0	MACS-02	2I	No. 2
0	1	MACS-03	2L	No. 3

Boards 1 and 2 each contain 16 pages, board 3 has 12 pages. The lowest four bits of PAR determine the specific page on the selected board.

The page address is loaded by an OUT 1=B instruction. The address enters the CIE Ancillary Board at 1Q and, after inversion, appears at the input to PADD, an 8-bit serial-in, parallel-out shift register. The address is clocked into PADD by CPO when enabled by OUT 1. After the eight CPO pulses, the end of the OUT 1 instruction, eight bits are contained in PADD; however, only the six least significant bits are

used for the page address and are applied to PAR. Also, the two least significant bits are routed to the NCU Ancillary Board via front plane connections 4T and 4S. Only two bits are required to permit page addressing of NCU Data Memory by the CIE because NCU Data Memory consists of only four pages. After completion of an OUT 1=B instruction, the address bits are strobed into PAR by the falling edge of PRESB at the clock input of PAR. PRESB is gated to the clock input provided DEV 1=64' is high. When DEV 1=64' is low, loading of PAR is inhibited but the loading of the page address into the corresponding NCU data memory page address register is enabled. That is, DEV 1=64 is routed to the NCU Ancillary Board via Front Plane connection 4U (see Figure 5-25, sheet 1) and PRESB' is routed to the NCU Ancillary Board via Front Plane connection 4R.

5.2.7.5 Data Input to Memory

Refer to Figure 5-25, sheet 3, for the following circuit descriptions.

The CIE Ancillary Board accepts an eight-bit data word (byte) from one of three sources: (1) The CIE B7*, (2) the Interface Board, or (3) the NCU Ancillary Board. If received from one of the first two sources, this word (byte) is then routed to one of two selected places: (1) The NCU Ancillary Board (and on to NCU Data Memory), or (2) the CIE Data Memory. If received from the NCU Ancillary Board, the byte can be routed only to the CIE Data Memory.

Data from the CIE B7* appears on the Data Out (DO) line, the input to MIR, and front plane connection 4Y (for routing to the NCU Ancillary Board). This data is clocked into MIR by CPO, when gated on by OUT 2. In order to send this data to the NCU Ancillary Board, the OUT 2 must be preceded by a DEV 1=32, or combination thereof. See Table 5-4 and the NCU Ancillary Board description in paragraph 5.2.6.

At the conclusion of the OUT 2 Instruction (eight clocks), the data word is contained in the MIR. The parallel outputs from MIR are then applied directly to the inputs of CIE Data Memory via the MIS's (Memory Input Switches). The MIS's act as switches connecting either of two inputs to their ourput. In effect, for MIS-1 and -2, the inputs are from either MIR or from the Interface Board. The input is selected by the state of the MIS select line which is established by DEV 1=2 (see Table 5-4). For example if DEV 1=2 is active (high), the selected input is from the Interface Board. Otherwise, it is from the CIE B7*.

The outputs of MIS-1 and -2 are connected to the inputs of MIS-3 and -4. The second input to MIS-3 and -4 is from the NCU Ancillary Board. The input selected is determined by this MIS's select line which is, in turn, established by DEV 1=16. That is, if DEV 1=16 is active (high), the selected input is from the output of MIS-1 and -2. Otherwise, it is from the NCU Ancillary Board.

While the outputs of MIS-3 and -4 are applied to the Data Memory inputs (MADI-10 thru MADI-17), a write pulse must be applied to memory control input (MAWRT'). This write pulse is generated by the one shot WRC. The pulse is also used to strobe data into the Interface Board's Buffer and the NCU Ancillary Board, when so directed. Pulse duration must be at least 400 ns (ideally 430 ns) to serve all those purposes. The Q output of WRC appears at C1 and is connected directly to the Interface Board via a flat interboard cable. This output is also routed to the CIE Data Memory via a NAND gate. Its application to the CIE Data Memory is inhibited whenever DEV 1-4, DEV 1=8, or DEV 1=32 is active (see Table 5-4). The Q' output of WRC is routed to the NCU Ancillary Board via Front Plane connection 4W, and is also used to clear flip-flop D7.

The input to WRC is actually the rising edge of the PRESB signal, gated in a number of ways. For writing directly to memory from the CIE B7*, i.e., via the OUT 2 instruction, the OUT 2' signal is inverted to a high and applied to the data input of flip-flop D7. The rising edge of PRESB occurs near the end of the OUT 2 Instruction and sets the flip-flop which serves as one enabling signal for gating PRESB to the WRC one shot. When OUT 2' is active, i.e., the CIE B7* is writing to its Data Memory, the signals identified as DEV 1=1', DEV 1=2', DEV 1=4', DEV 1=8', and DEV 1=16' are all inactive (high). Hence, PRESB is gated to the input of WRC, and the output of WRC occurs after the last clock pulse of the OUT 2 instruction. Similarly, when any one or more of the signals identified as DEV 1=2', DEV 1=4', DEV 1=8', and DEV 1=16' is active (low), the DEV 1=1' is inactive (high), then PRESB is gated to WRC, via NAND gate A7. Therefore, when OUT 2' is inactive, but any of the DEV signals other than DEV 1=1' is active, a WRC output pulse will occur for each rising edge of PRESB. When DEV 1=1' is active (low), it inhibits WRC action. However, the DEV 1=1' condition is set only to terminate an NCU to CIE parallel transfer. See Table 5-4.

5.2.7.6 Data Output from Memory

Refer to Figure 5-25, sheet 4, for the following circuit descriptions.

The CIE Ancillary Board accepts an eight-bit parallel data word (byte) from one of two sources: (1) The CIE Data Memory, or (2) the NCU Data Memory, via the NCU Ancillary Board. If received from the CIE Data Memory, this word is then routed to one of three selected places: (1) The Interface Board, (2) NCU Data Memory, via the NCU Ancillary Board, or (3) the CIE B7*. If received from the NCU Data Memory, via the NCU Ancillary Board, it can be routed only to the CIE B7*. Figure 5-25, sheet 4, shows these alternatives.

Data from the CIE Data Memory appears on the input lines identified as MPDO 10' (MSB) thru MPDO 17' (LSB). These eight lines are multipled to three sets of connections: (1) The Interface Board via backplane connections (not shown on Figure 5-25, sheet 4), (2) MORS-1 and MORS-2 for routing to the CIE B7*, and (3) Front Plane connections 3G through 3N, for connections to the NCU Ancillary Board. (Note that a pull-up resistor must be associated with each of the eight data lines.) For transfer of data to the Interface Board, a DEV 1=4 condition must be set. See Table 5-4. A word will then be transferred for each incrementation of the MAR. See preceding section on Word Addressing. For transfers of data to the NCU Ancillary Board, a DEV 1=8 condition must be set. Again, a word will be transferred for each incrementation of the MAR. For transfer of data to the CIE B7*, a DEV 1=32 condition must not be set, i.e., DEV 1=32' is inactive or high. This will result in the data being routed through switches MORS-1 and -2 to the inputs of the Memory Output Register (MOR). When DEV 1=32 is set (DEV 1=32' is low), the switches route the second set of inputs from the NCU Data Memory, via the NCU Ancillary Board, to the inputs of MOR. In either case, the data present on the MOR inputs must be loaded into MOR. This is accomplished by the load pulse ($\approx$65 ns) generated by the MOR OS (E3). This pulse results from triggering the OS with the rising edge of BEX 1 while PRESB' is low. Hence, the rising edge of BEX 1 causes MOR to be loaded, and the eight clock pulses (CPO) that occur while BEX 1 is high are gated to the clock input of MOR. Thus, the parallel data input to MOR is shifted out serially to the B-Register of the CIE B7*. This data is routed from pin 3V via the NCU Ancillary Board and is further described in its documentation. See Figure 5-22, sheet 5, of NCU Ancillary Board and accompanying text in paragraph 5.2.6.6.

5.2.8 LOOP INTERFACE UNIT (LIU)

The Loop Interface unit provides the capability of interfacing the NCU to the actual Transmission Loop or Bus (see Figures 5-27 and 5-28). The operation of the LIU is described in the following subsections: (1) Bus interface, (2) B7* interface and, (3) B7* interface to Bus interface.

5.2.8.1 Bus Interface

The Bus interface provides the necessary Bus receiver and driver, also the required logic to separate clock and data from the bit stream. In addition, the interface provides internal timing control, clocks and data to the B7* processor, and regenerates clocks and data for the Bus.

5.2.8.1.1 Bus-In Delayed

Bus-In is received on the LIU board by a Bus receiver. The Bus-In Delayed logic, shown in Figure 5-27, sheet 1, provides a standardized, noise-free Bus input to the LIU card. Bus-In Delayed (BID) is used throughout the LIU board as the Bus input. Clock to Bus-In Delayed (CBID) provides a pulse with each Bus transition and strobes the Bus-In into the BID flip-flop. It is also used to generate the internal timing which is described in paragraph 5.2.8.1.2. The relationship among Bus-In, CBID, BID, and a 1 MHz reference is shown in Figure 5-27, sheet 1.

5.2.8.1.2 Internal Timing Generation

All internal timing on the Node board is derived from the four monostable multivibrators shown in Figure 5-27, sheet 2. These timing waveforms are directly related to the actual loop data rates, and since the loop rates are selectable to the extent that a high, medium, or low rate is available, these timing waveform rates must be similarly selectable. This capability is provided via the capacitors and switches associated with one shots G5 and G3. The trimmer capacitors are adjusted with the switch in the high-speed position. Adjustment should be made to achieve a 700-750 nsec positive pulse width at G5 pin 8, and a 400-500 nsec positive pulse width at G3 pin 8.

T1 is triggered by every clock transition. For the High-Speed Switch setting it is a 750 nsec pulse which spans across each potential data transition. T1 is self-synchronizing to the byte in that a missing clock transition occurs during the control (C) and data (D) indications. This assures that T1 will be reset when the first transition of the next byte, which is always a clock transition, appears.

T2 is triggered by the trailing edge of T1 and provides a 500 nsec pulse, for the High-Speed Switch setting, which is used as a reference for retiming the output bus. Essentially, the rising edge of T2 indicates a clock transition and the trailing edge a possible data transition for bus out.

T3 is a 40 nsec pulse which is triggered by the trailing edge of T2. It is used to provide any necessary data transition for the bus out.

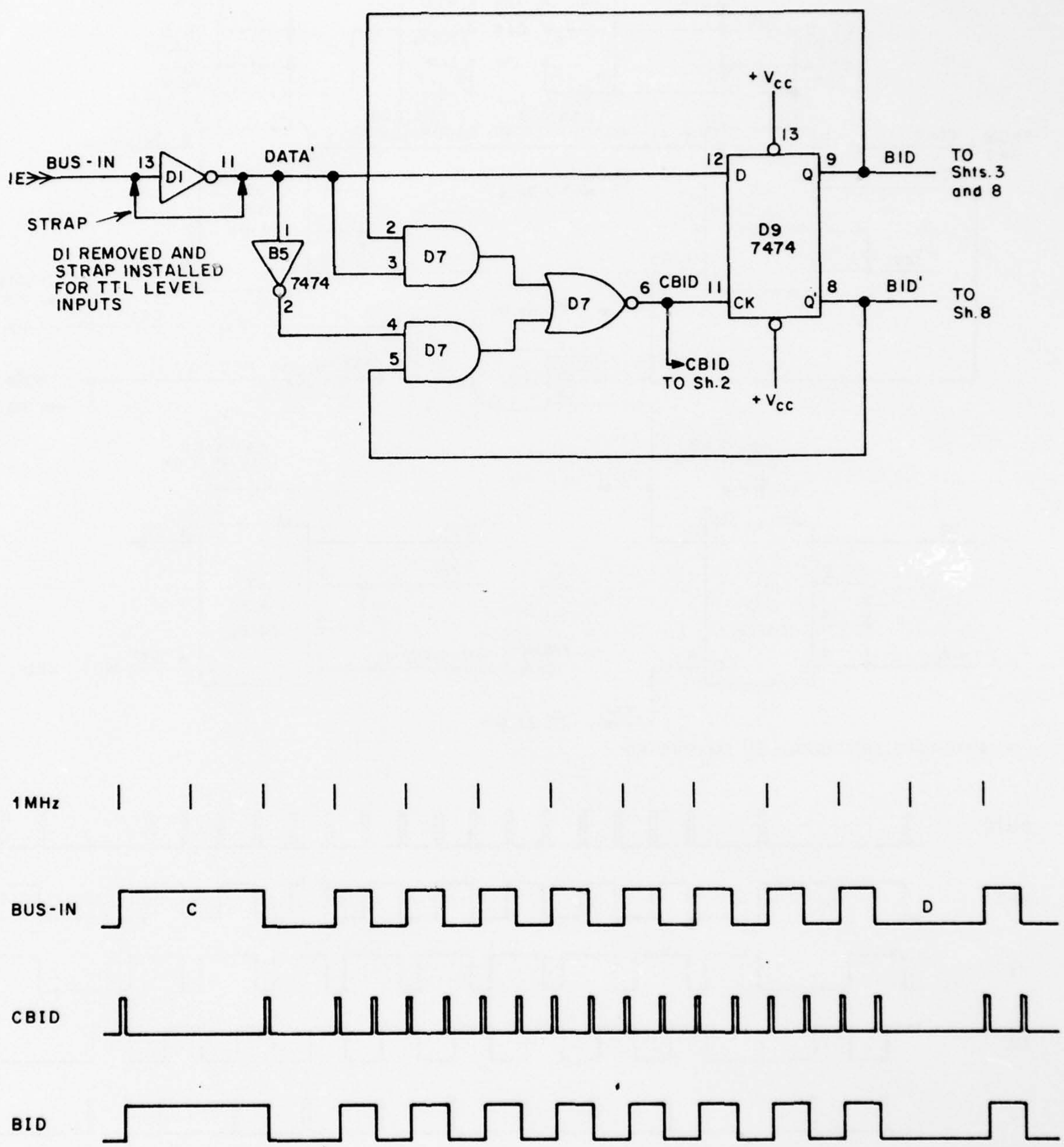


Figure 5-27. Loop Interface Unit Logic (Sheet 1 of 9)

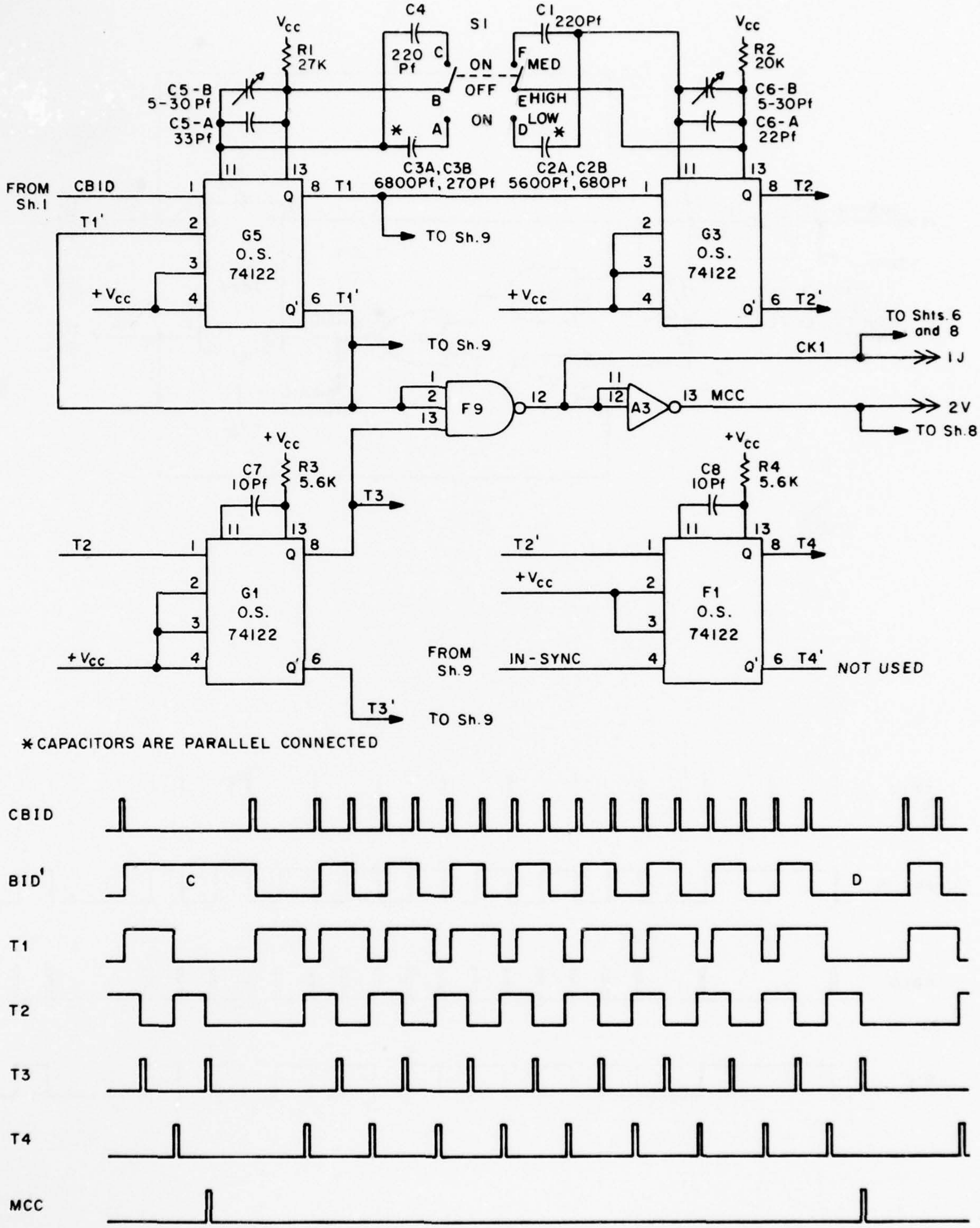


Figure 5-27. Loop Interface Unit Logic (Sheet 2 of 9)

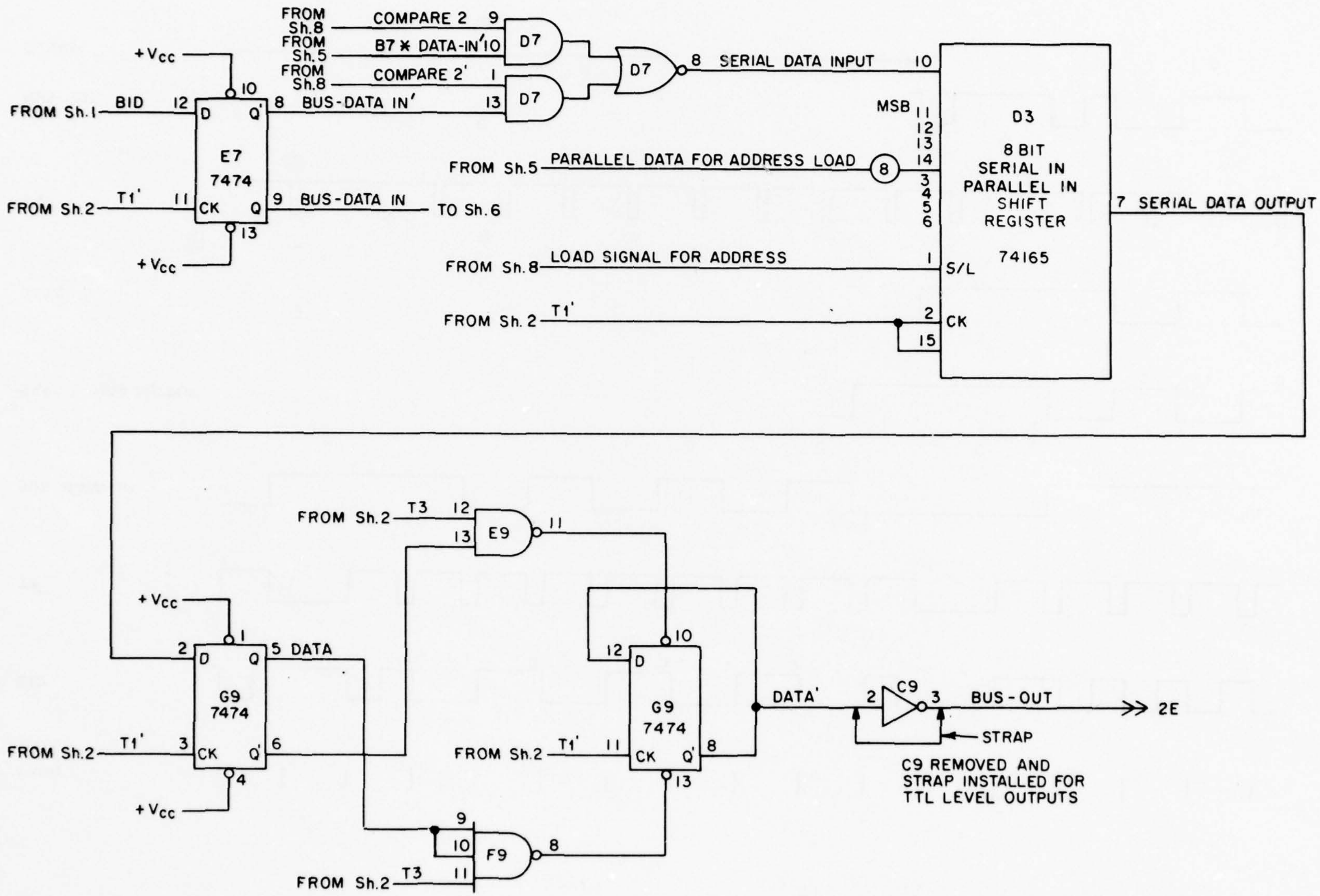


Figure 5-27. Loop Interface Unit Logic (Sheet 3 of 9)

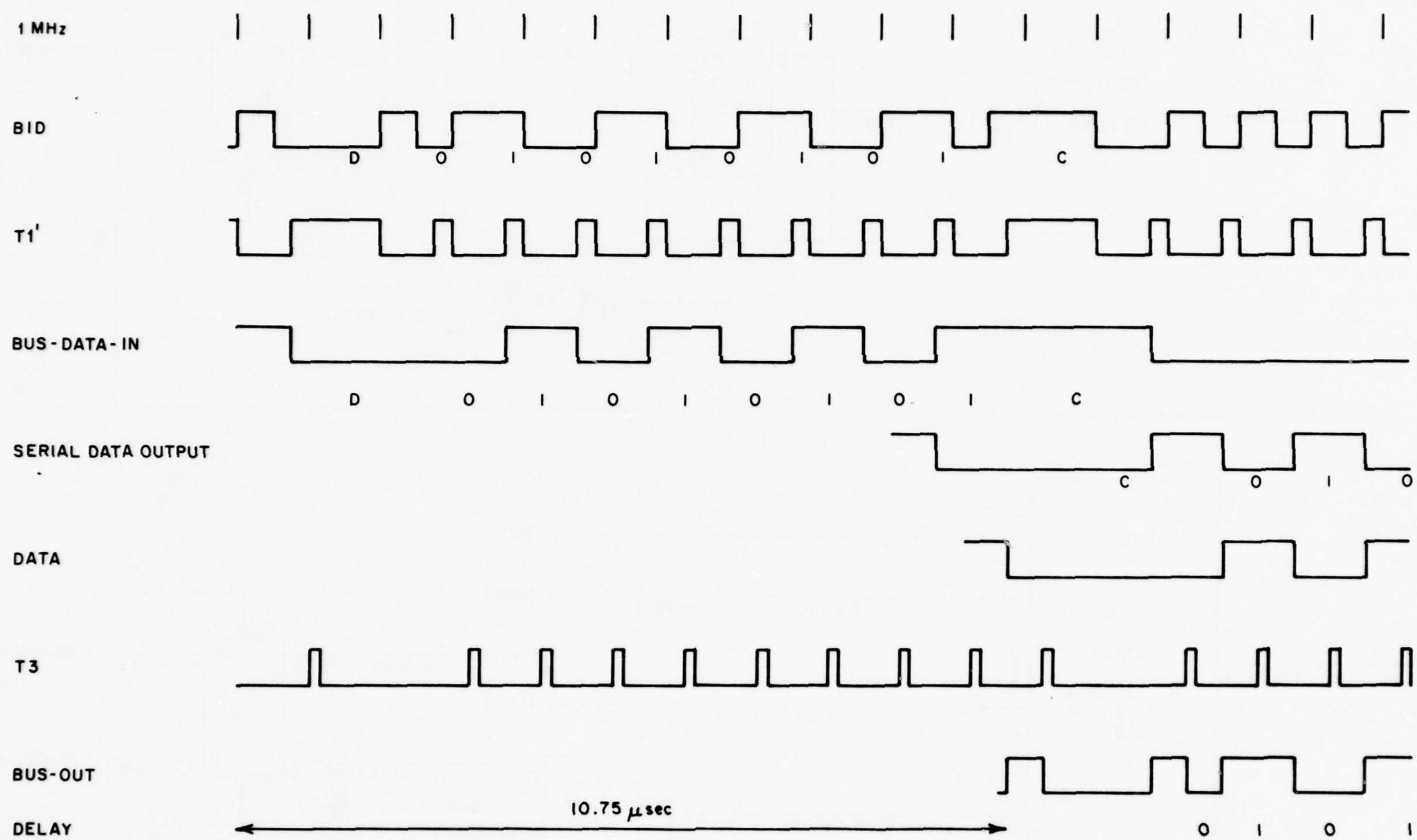


Figure 5-27. Loop Interface Unit Logic (Sheet 4 of 9)

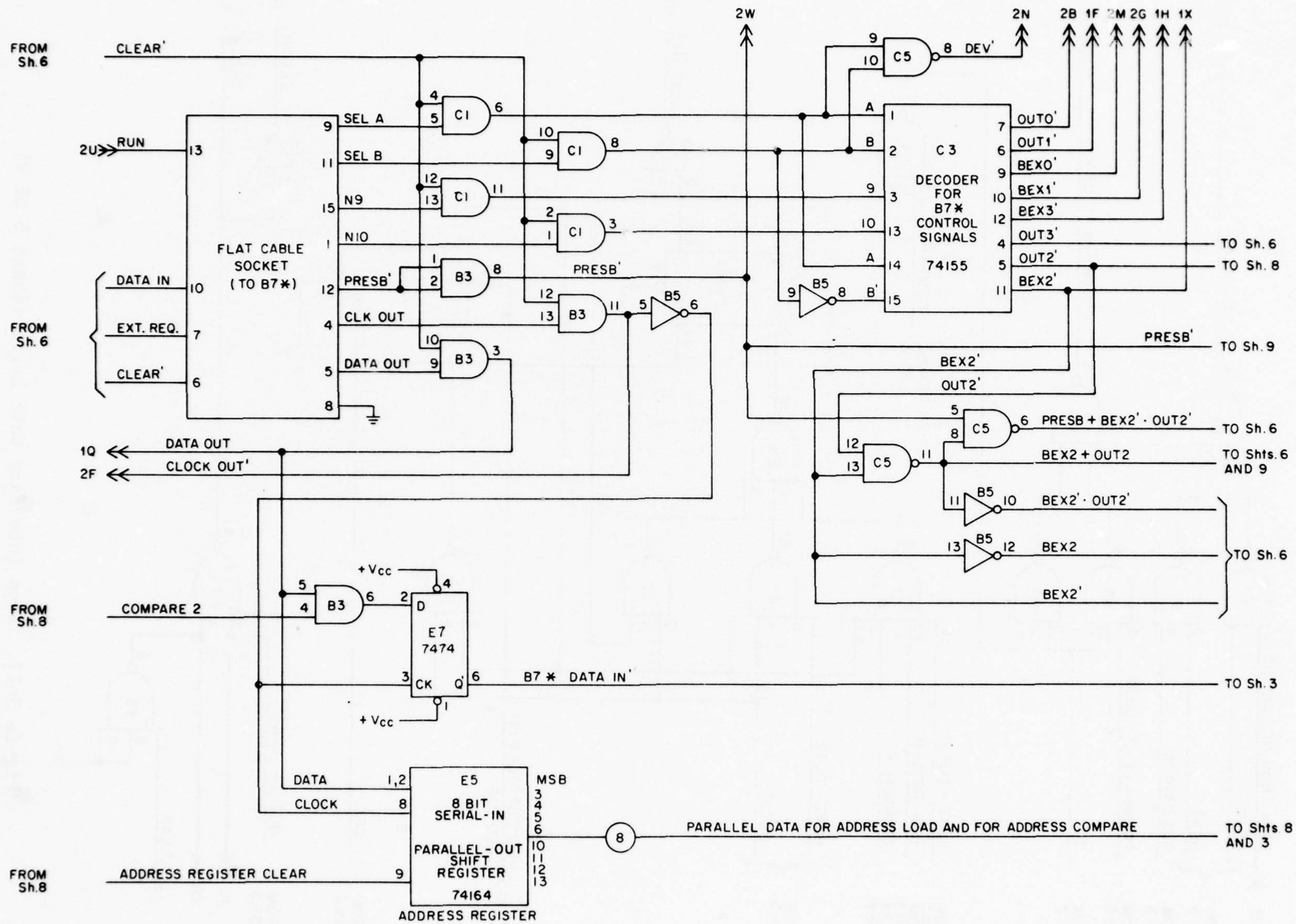


Figure 5-27. Loop Interface Unit Logic (Sheet 5 of 9)

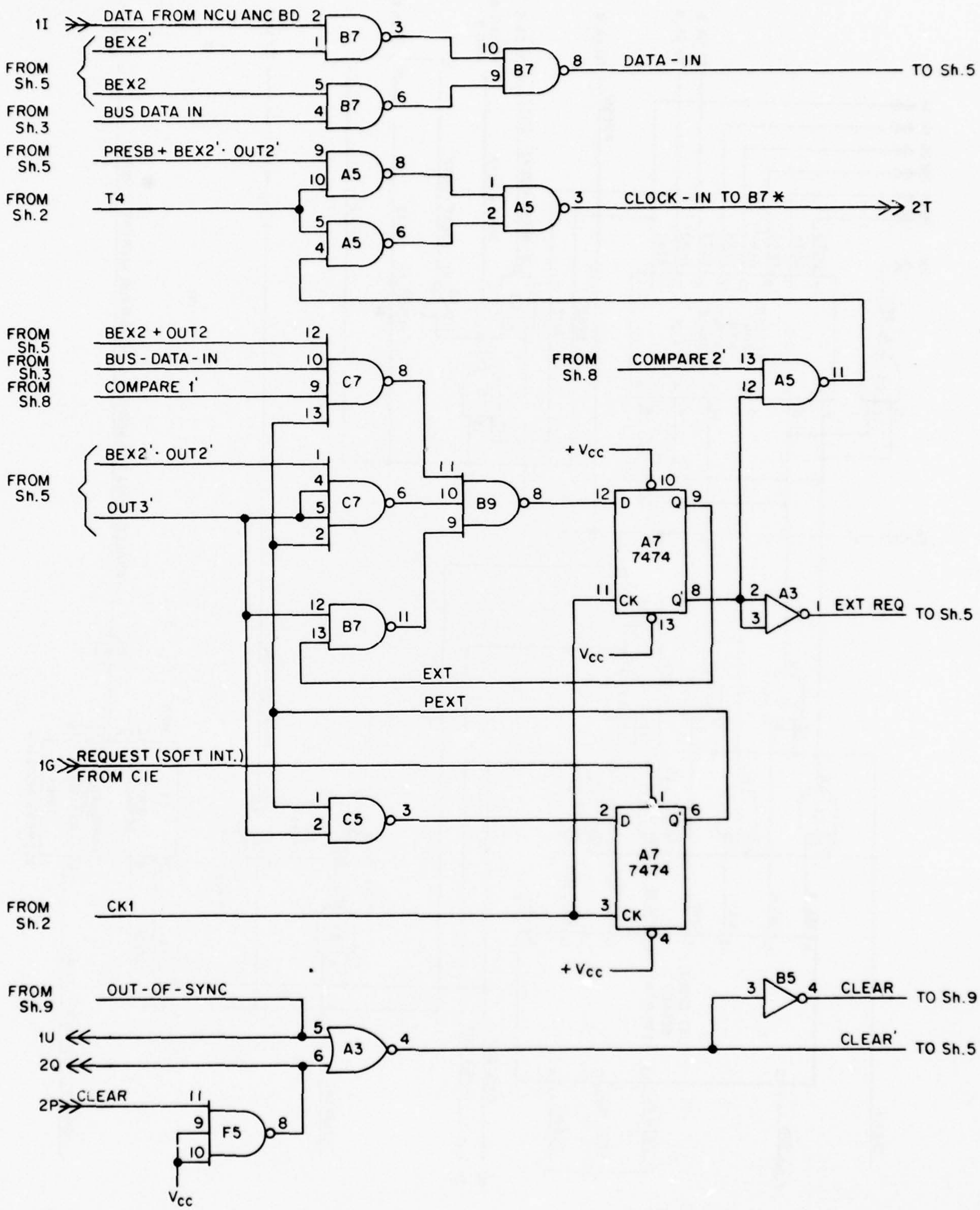


Figure 5-27. Loop Interface Unit Logic (Sheet 6 of 9)

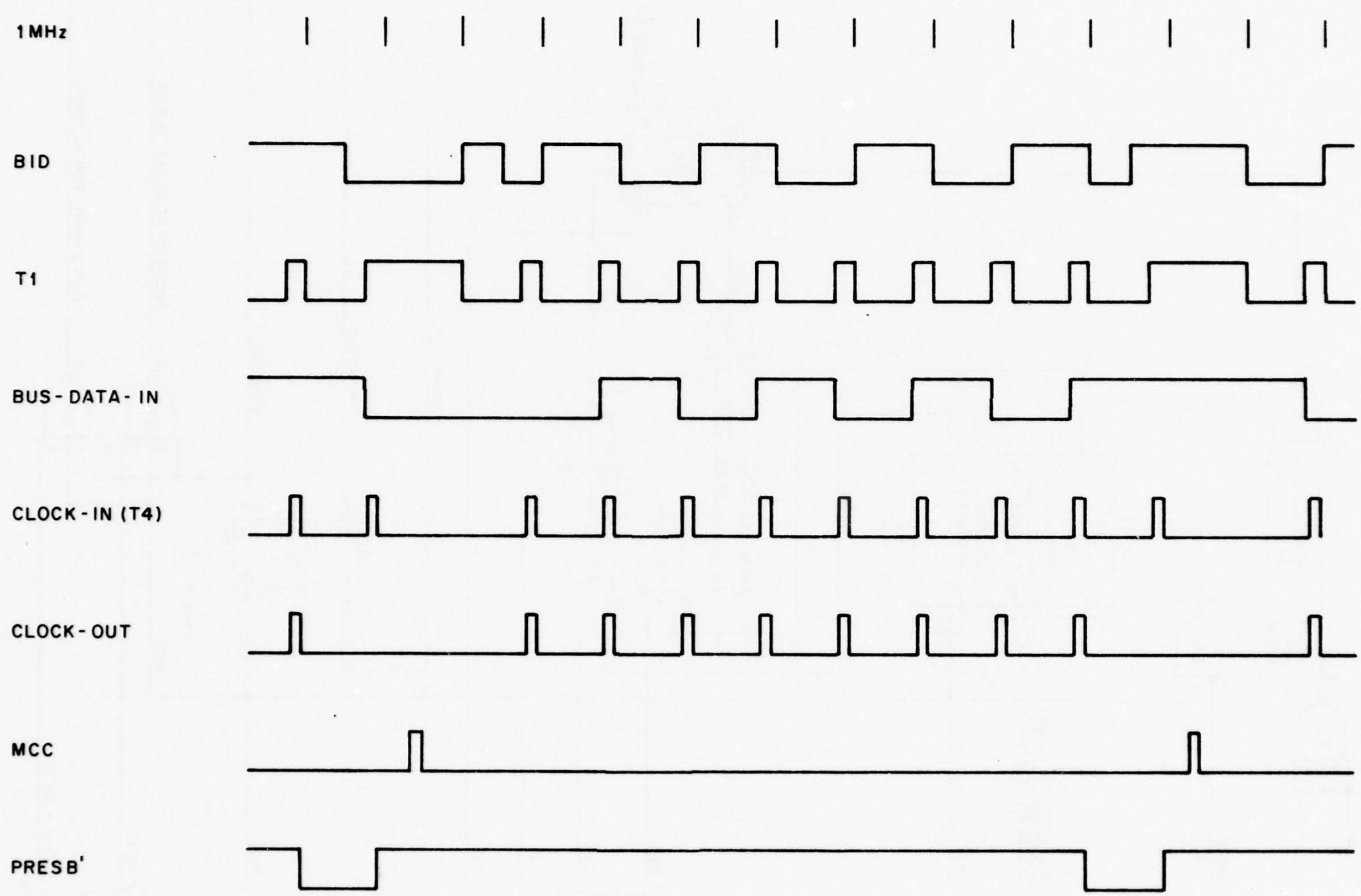


Figure 5-27. Loop Interface Unit Logic (Sheet 7 of 9)

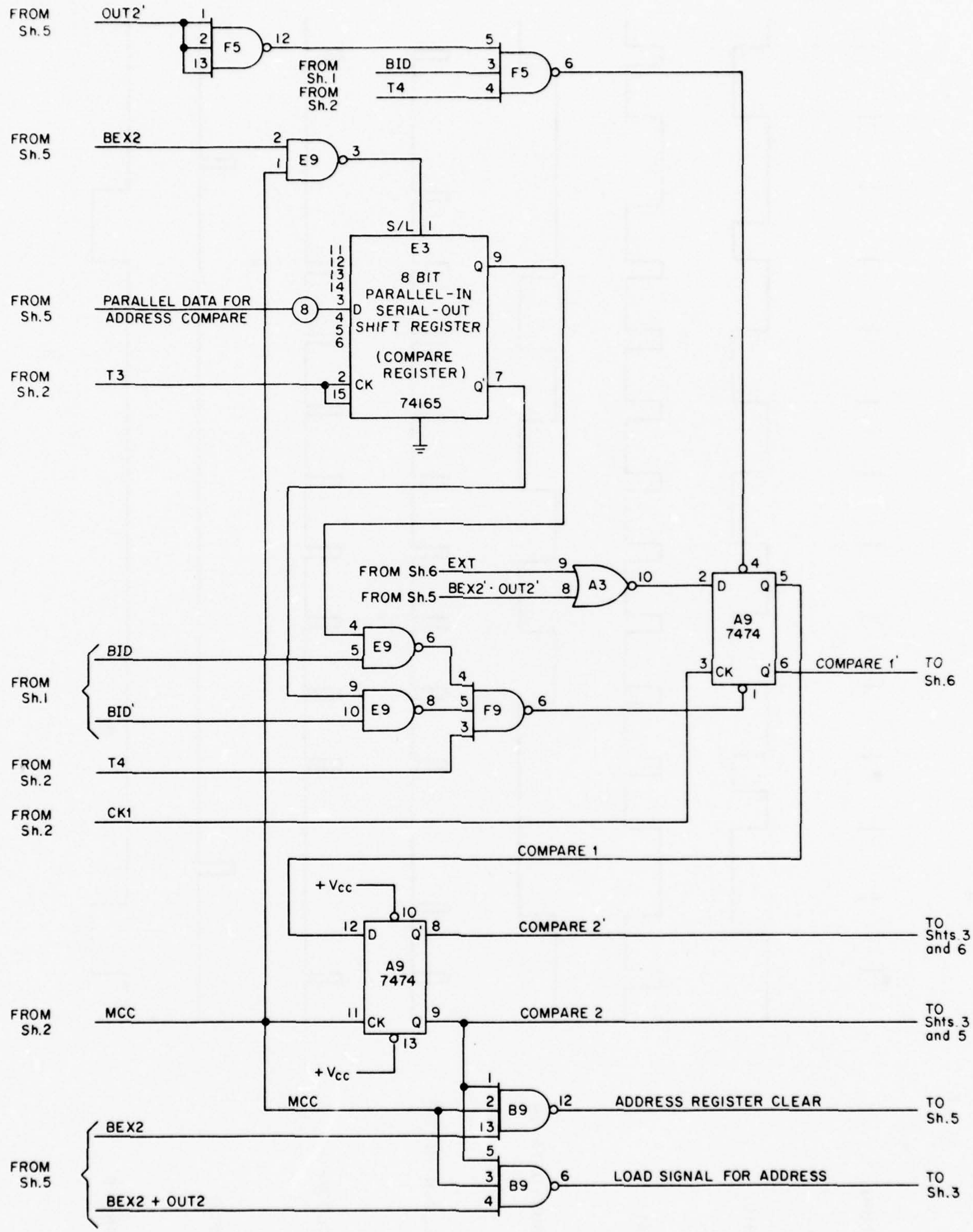


Figure 5-27. Loop Interface Unit Logic (Sheet 8 of 9)

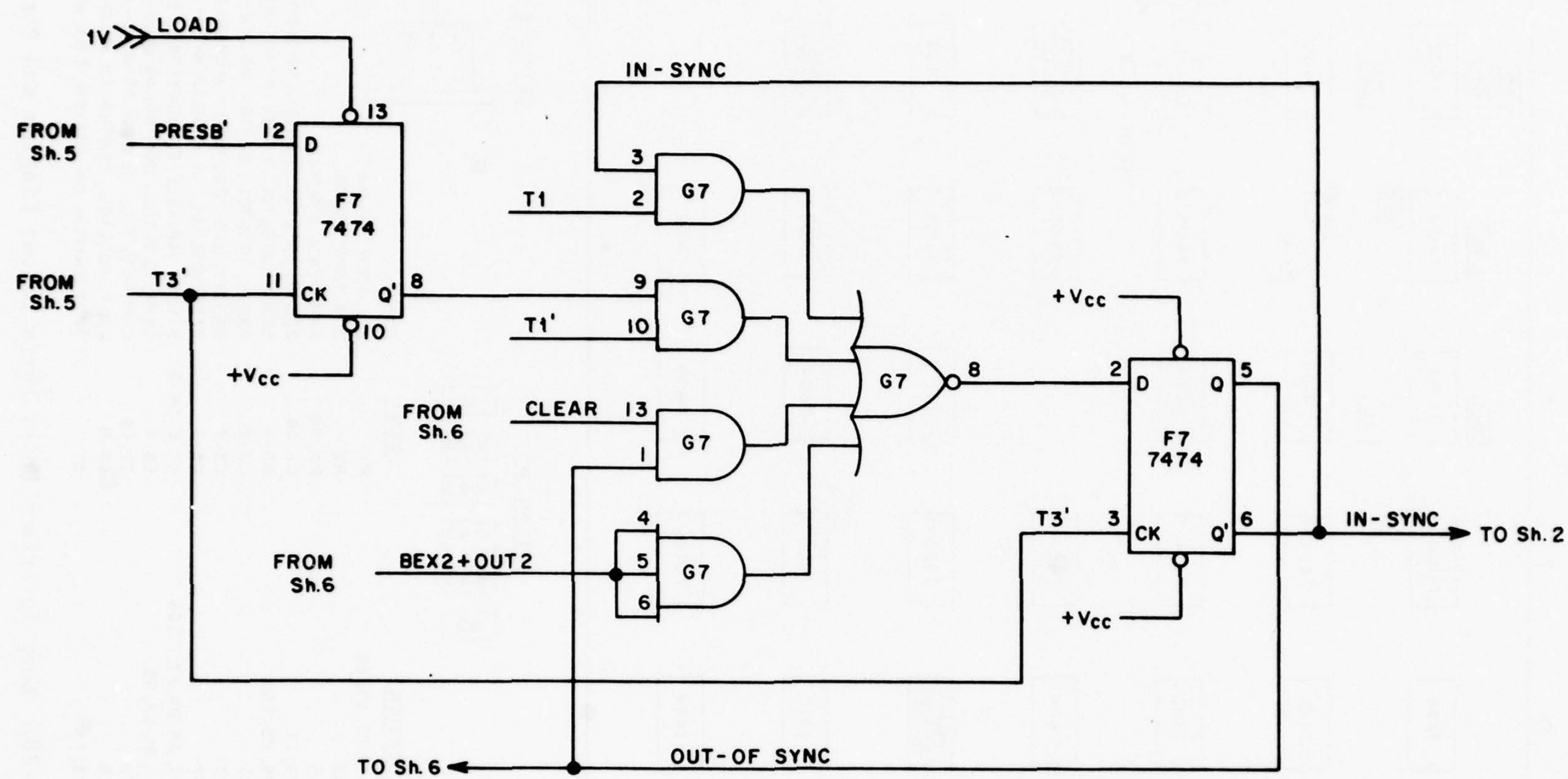
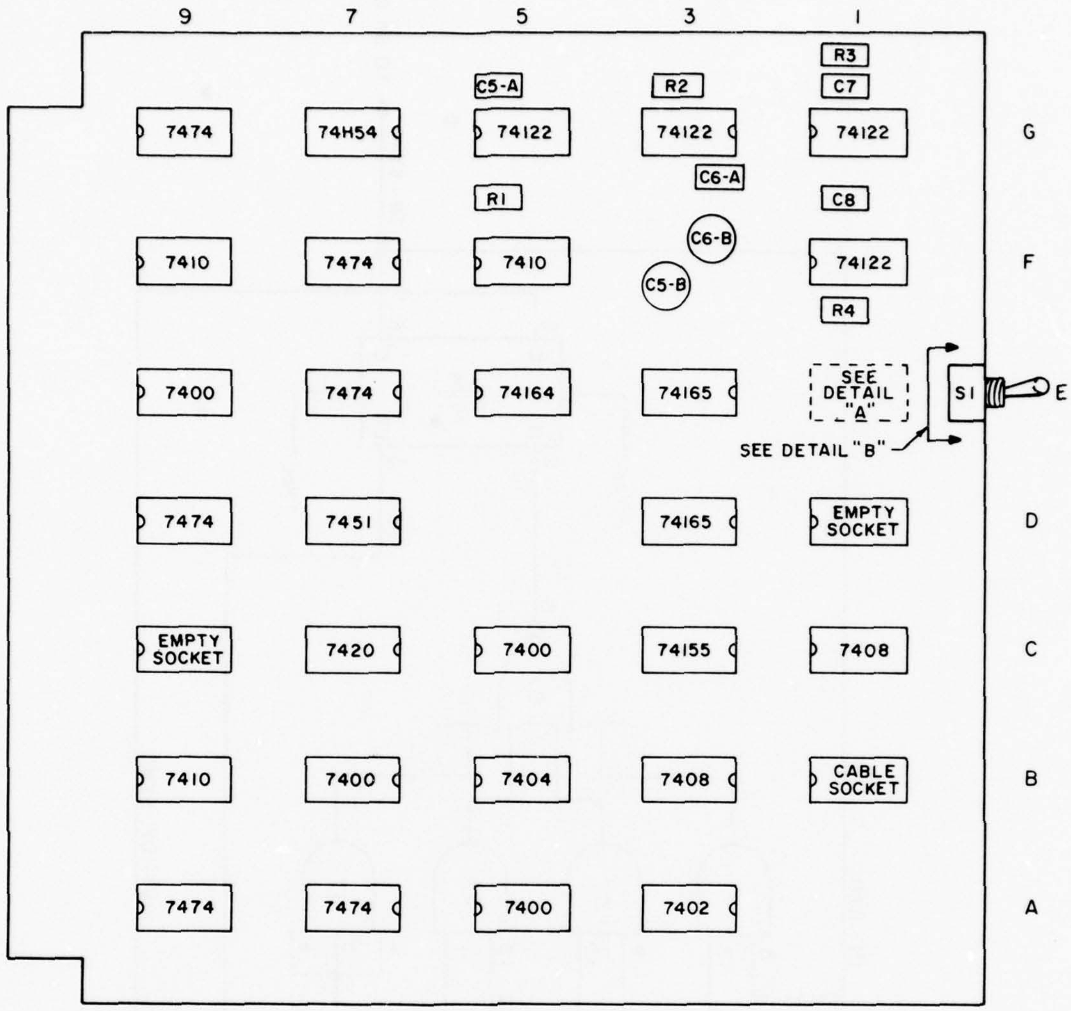
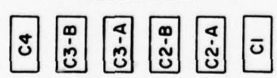


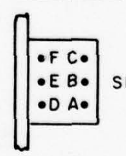
Figure 5-27. Loop Interface Unit Logic (Sheet 9 of 9)



DETAIL "A"



DETAIL "B"



IDENT	LOCATION
7400	A5, B7, C5, E9
7402	A3
7404	B5
7408	B3, C1
7410	B9, F5, F9
7420	C7
7451	D7
74H54	G7
7474	A7, A9, D9, E7, F7, G9
74122	F1, G1, G3, G5
74155	C3
74164	E5
74165	D3, E3

IDENT	VALUE
R1	27K, 1/8W, 5%TOL.
R2	20K, 1/8W, 5%TOL.
R3, R4	5.6K, 1/8W, 5%TOL.
C1, C4	220 Pf, 10%TOL., CENTRALAB #DD-221
C2-A	5600 Pf, 10%TOL., KEMET #CK05-BX-562K
C2-B	680 Pf, 10%TOL., CENTRALAB #DD-681
C3-A	6800 Pf, 10%TOL., KEMET #CK05-BX-682K
C5-A	33 Pf, 10% TOL., CENTRALAB #DD-330
C5-B, C6-B	5-30 Pf VARIABLE, E.F.JOHNSON #275-0430-005
C6-A	22 Pf, 10% TOL., CENTRALAB #DD-220
C7, C8	10 Pf, 10% TOL., CENTRALAB #DD-100
C3-B	270 Pf, 10%TOL., CENTRALAB #DD-271
S1	DPDT SWITCH, ON-OFF-ON, C&K #7203-SYZQ

Figure 5-28. Loop Interface Unit, Parts Layout Diagram and Parts List

T4 is also a 40 nsec pulse which is triggered by the leading edge of T2. It is used primarily as the clock input to the NCU B7*. The signal In-Sync permits T4 to be triggered only when the bus is in sync with the NCU B7*. If the two entities get out of sync, clocks will be inhibited from going into the B7*. The sync circuitry will be described in detail in paragraph 5.2.8.3.3.

MCC is a 40 nsec pulse occurring once every time slice during a control or data designation. It is used to clear registers and set up control flip-flops prior to the execution of the next B7* command.

5.2.8.1.3 Bus Delay and Retiming

Bus-In is passed through a total of 12 flip-flops in the node. The first flip-flop, BID, is discussed in paragraph 5.2.8.1.1. The remaining 11 are shown in Figure 5-27, sheet 3, and the associated timing diagram is shown in Figure 5-27, sheet 4. Note that D3 represents eight flip-flops.

Data is extracted from the Bus at T1' time by the Bus-Data-In flip-flop. The serial data input to the shift register carries data from the Bus, or data from the B7*. The Compare 2 flip-flop, Figure 5-27, sheet 8, determines the input to the shift register. For the purpose of this discussion, assume that the Compare 2 flip-flop is in the state to permit data from the Bus. Data flows through the eight bits of the shift register and the Data flip-flop on the rising edge of T1'. Bus retiming occurs on the last flip-flop of the chain. The rising edge of T1' causes a clock transition, and the rising edge of T3 causes a possible data transition based on the state of the Data flip-flop. The total delay from the input of BID to the output on Bus-Out is 10.75 μsecs, as shown in Figure 5-27, sheet 4.

5.2.8.2 NCU B7* Interface

The NCU B7* interface provides the necessary input signals to the B7*, and the necessary decoders and drivers for the output signals. The input signals include Clock-In, Data-In, External Interrupt, and Clear. Outputs from the B7* encompass the Clock-Out, Data-Out, Preset B´, A, B, N9, and N10 signals.

5.2.8.2.1 NCU B7* Outputs

The B7* outputs, shown in Figure 5-27, sheet 5, illustrate the decoders and registers associated with the B7* outputs. All outputs from the B7* are buffered before going to the logic. Control signals A, B, N9, and N10 are used to generate the I/O control signals: OUT 0´, OUT 1´, OUT 2´, OUT 3´, BEX 0´, BEX 1´, BEX 2´, BEX 3´, and DEV´. OUT 2´, OUT 3´ and BEX 2´ are used on the LIU board to designate a Bus Write, Interrupt Reset, and Bus Read. The remaining decodes, as well as PRESB´, Clock-Out´, and Data-Out, go off the board for external use.

The B7* Data-In flip-flop provides the one-bit time delay which is necessary to synchronize the B7* data with the bus data. The output of the flip-flop goes to Figure 5-27, sheet 3, and is permitted to flow into the eight-bit serial-in, parallel-in shift register as data for the bus whenever the COMPARE 2 control flip-flop has been set.

On Figure 5-27, sheet 5, data from the B7* is clocked with Clock-Out to fill the eight-bit shift register. Its output is used as parallel data for Address Load, shown on Figure 5-27, sheet 3, and for parallel data for address compare shown on Figure 5-27, sheet 8. Various combinations of BEX 2 and OUT 2 are provided by C5 on Figure 5-27, sheet 5, as control signals for use throughout the LIU board.

5.2.8.2.2 NCU B7* Inputs

NCU B7* inputs are shown in Figure 5-27, sheet 6, and the associated timing diagram is shown in Figure 5-27, sheet 7. Data-In to the B7* at B7-8 comes from Bus-Data-In during a BEX 2 instruction, or from an external source (B7-2) during a BEX 0, BEX 1, or BEX 3 instruction. Clock-In (A5-3) occurs at T4 time. Clock-In is permitted on any instruction which is in sync, and does not specify an OUT 2 command or BEX 2 command. During OUT 2 and BEX 2 the clocks are gated via A5-4 into the B7* if the desired address compare has occurred. External request at pin 1G also permits the clocks to be gated into the B7*. The external request flip-flop (A7) is synchronized with the bus, via clock CK1, in order to prevent erroneous data from being inserted or extracted from the bus. B7* Clear (A3-4) may be driven from three external sources, via inputs 1U, 2Q, and 2P.

5.2.8.3 <u>NCU B7* Interface to Bus Interface</u>

Data extraction and data insertion relative to the Bus occur during a Bus Read operation and Bus Write operation, respectively. The controls for the B7* interface to bus interface are shown in Figure 5-27, sheet 8, and are described as applicable during the description of Bus Read and Bus Write.

5.2.8.3.1 Bus Read

A Bus Read operation is initiated by a sequence of instructions in the NCU B7*. An example of this sequence is:

```
A1    =  A1
BEX 2  A2 = A2
IF EXT SKIP
GO TO EXCEPTION
```

The first instruction, A1 = A1, loads the eight-bit serial-in Address Register (E5) shown in Figure 5-27, sheet 5, with the data contained in the A1 register. The second instruction, BEX2 A2 = A2, signals the Loop Interface Unit to start a Bus Read operation, and clocks to the B7* are inhibited (via A5-9). See Figure 5-27, sheet 6. The compare register (E3), shown in Figure 5-27, sheet 8, is loaded with the address in the Address Register (E5). The Compare 1 flip-flop is set, and a bit-by-bit compare of the register with the data on the bus is initiated. If any bit of data does not compare, or a data field is detected, the Compare 1 flip-flop is reset. If a match occurs, i.e., a control field which contains the desired address, the Compare 2 flip-flop is set, causing a series of events. The control field is forced to zero thus indicating a blank time slot. Clocks are restored to the B7* thereby permitting the execution of the BEX 2 instruction.

5.2.8.3.2 Bus Write

The Bus Write operation is also initiated by a sequence of B7* instructions. An example is:

```
A1    = A1
OUT 2 = A2
```

The first instruction, A1 = A1, places the address contained in the A1 register of the B7* into the eight-bit serial-in, parallel-out shift register (Address Register-E5) shown in Figure 5-27, sheet 5. The second instruction, OUT 2 = A2, causes the LIU logic to initiate a search for a time slot. Upon the receipt of an OUT 2 command, the LIU logic inhibits (via A5-9) the clock into the B7*, as shown on Figure 5-27, sheet 6, resets the eight-bit parallel-in serial-out compare register (E3) as shown on Figure 5-27, sheet 8, sets the Compare 1 flip-flop (A9), and initiates a bit-by-bit comparison of the information on the bus. Whenever a control byte is detected, the eight-bit serial-in, parallel-in shift register in Figure 5-27, sheet 3, is parallel loaded with the address. Clocks are then restored to the B7* and the output data from the B7* is permitted to flow into the serial-in, parallel-in shift register (D3) in Figure 5-27, sheet 3, thus placing data on the bus.

5.2.8.3.3 B7*/Bus Sync Control

The B7*/Bus Sync Control Logic is shown in Figure 5-27, sheet 9. It is used primarily during system initiation when the clear signal is active. The purpose of this logic is to assure that the nine clocks which are presented to the B7* occur during the nine data portions of each time slice. If this condition does not occur during initiation of the system, this logic provides an automatic means of achieving sync. During normal execution, the IN-SYNC line should always be active (a low at F7, pin 6). The line will become non-active and inhibit clocks to the B7* only if an abnormal condition occurs which would put the Bus and B7* out of Sync with respect to each other.

5.2.9 HOST INTERFACE BOARD

The Host Interface Board, together with an M1710-modified board, described in paragraph 5.2.10, permits an ESM CIE to interface a PDP-11/40 Host Processor on a serial transmission basis (see Figures 5-29 and 5-30). In this configuration, ASCII characters (seven bits plus parity) are exchanged in a synchronous mode at 560 Kilobits per second. Each exchange involves a packet of data comprising 256 characters, or 128 sixteen-bit words.

The Host Interface Board consists of: (1) An Output Packet Buffer, with respect to the Host; (2) an Input Packet Buffer, with respect to the Host; and (3) a Buffers Status Register. It also provides for interfacing the data and clock lines from the Host to the ESM Loader Boards.

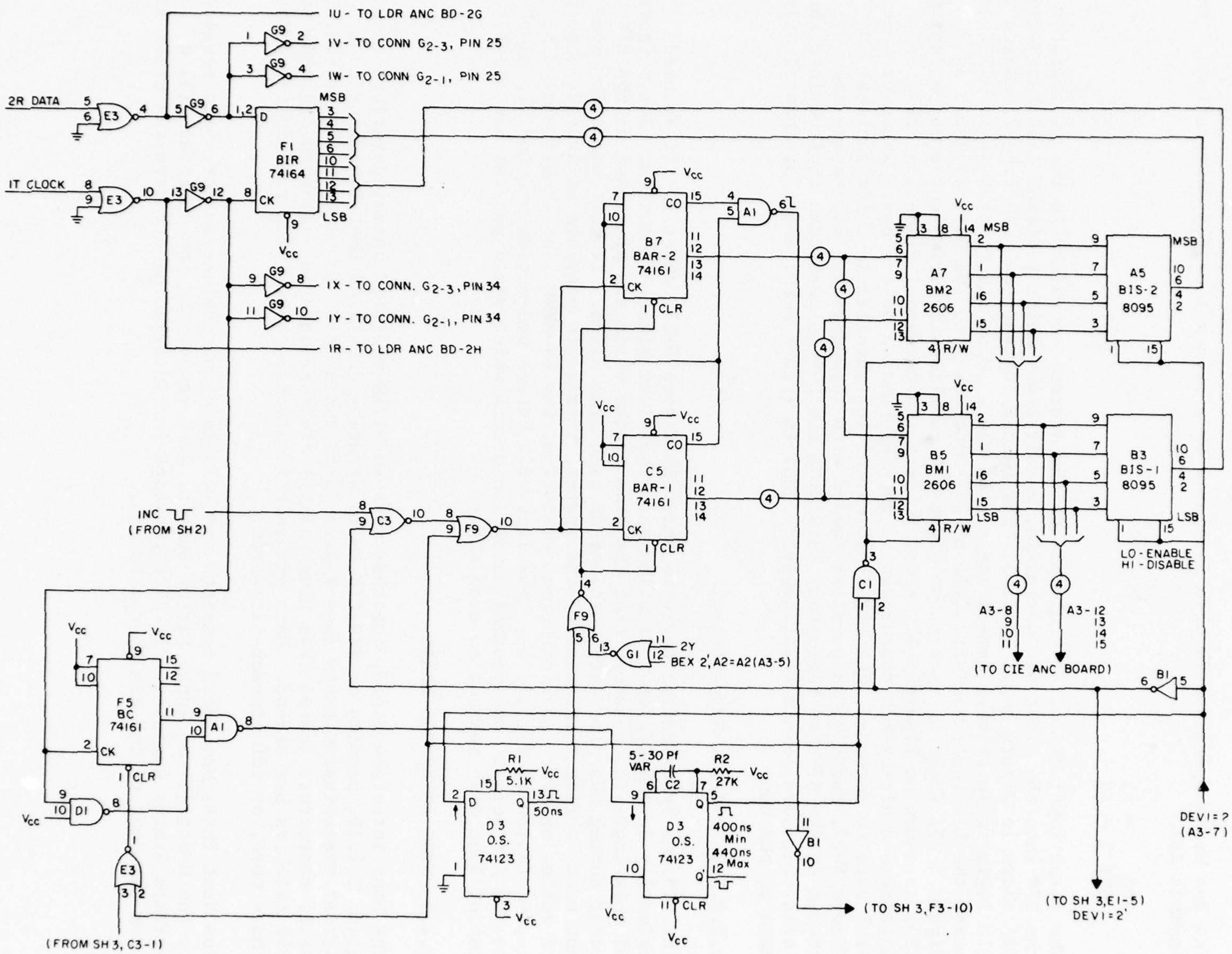


Figure 5-29. Host Interface Board Buffer Logic (Sheet 1 of 3)

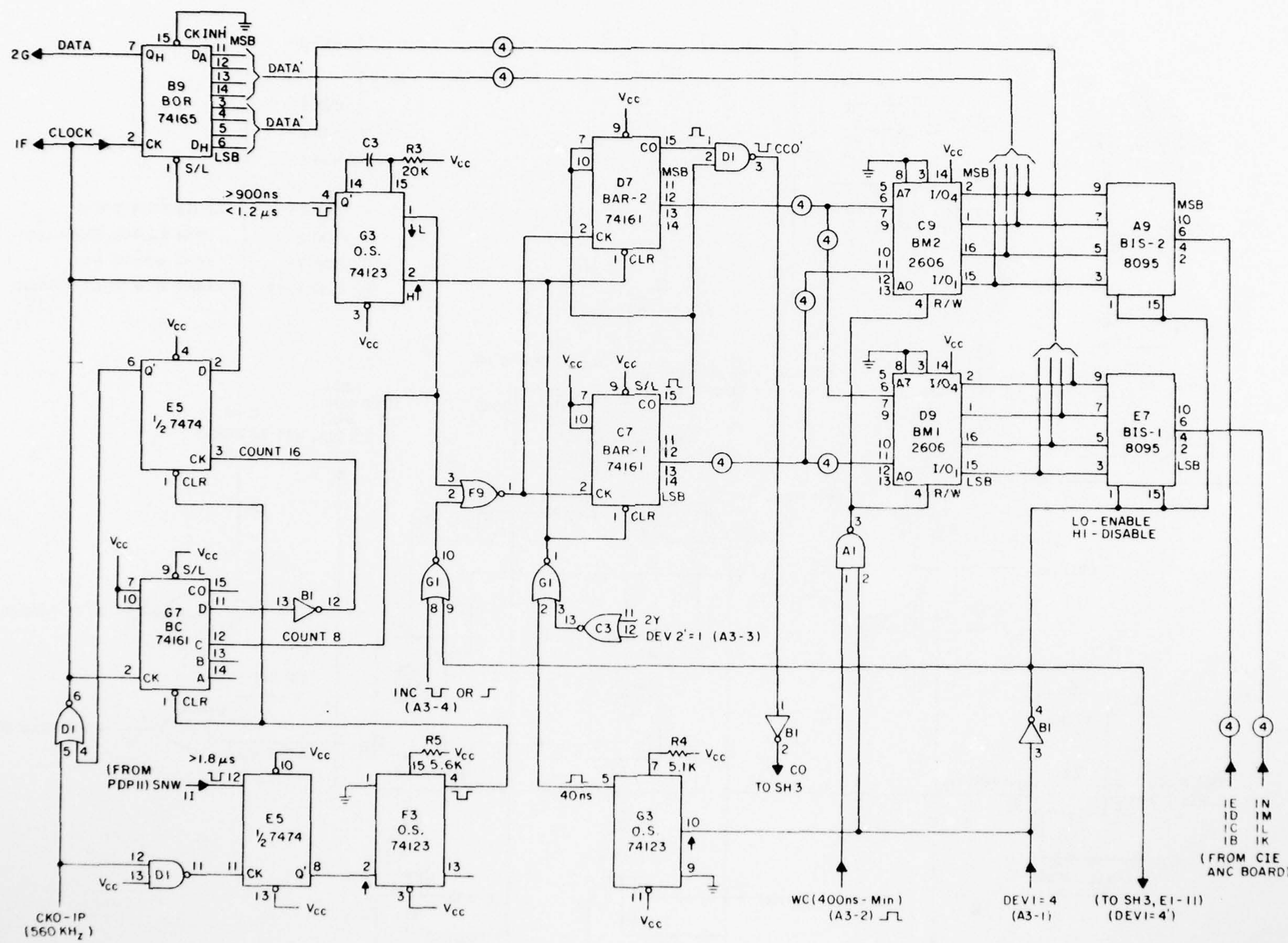


Figure 5-29. Host Interface Board Buffer Logic (Sheet 2 of 3)

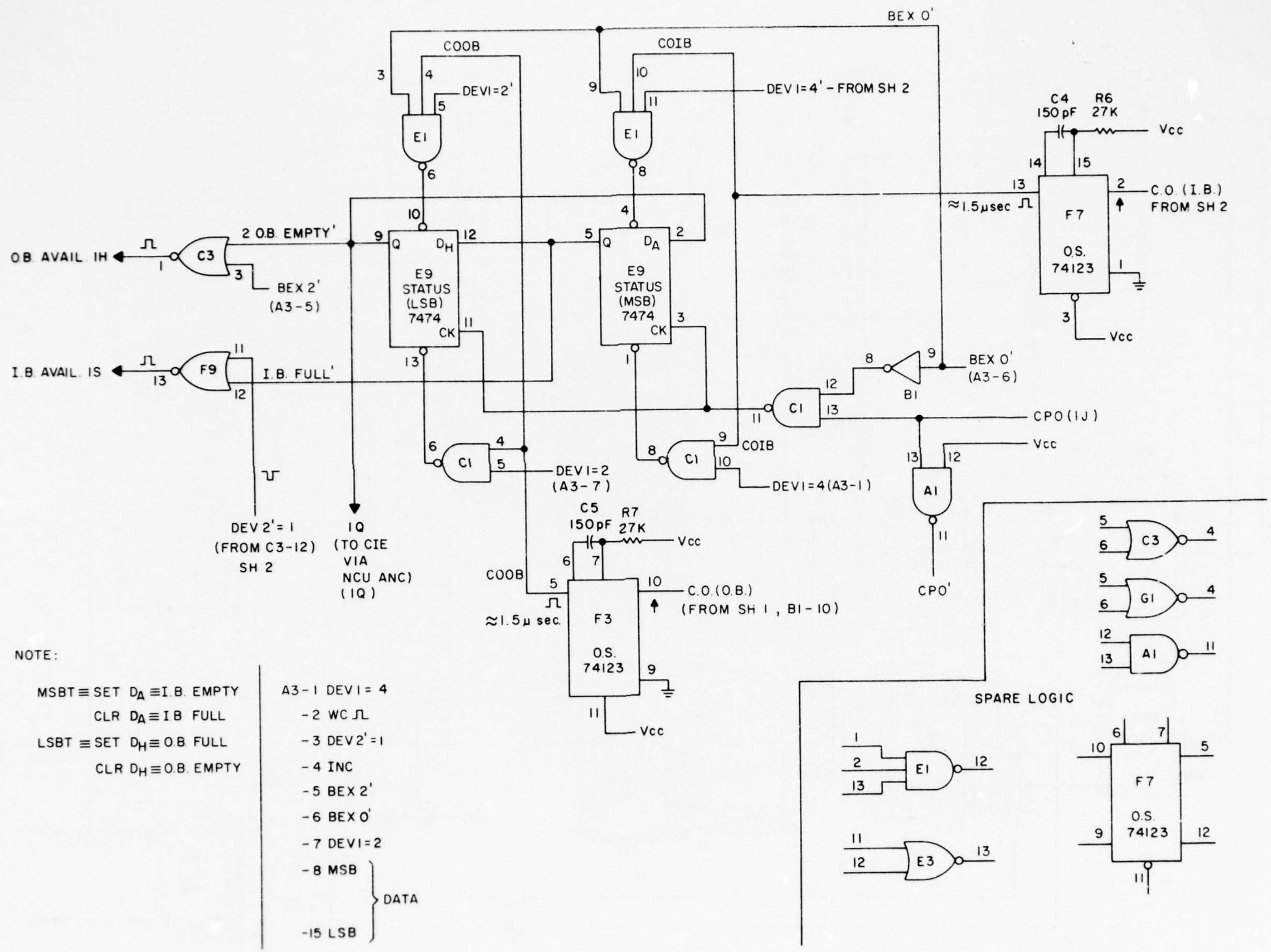
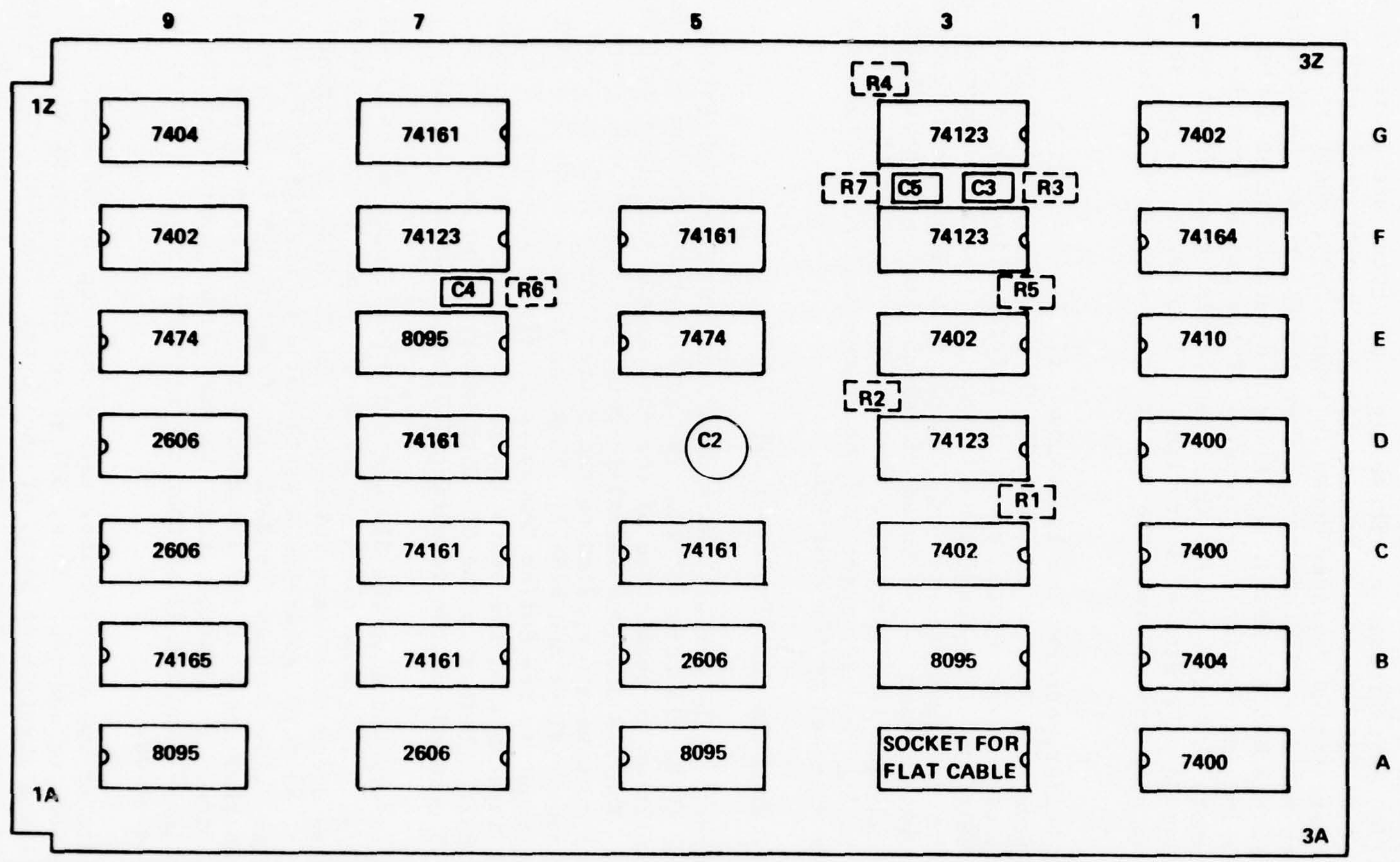


Figure 5-29. Host Interface Board Buffer Logic (Sheet 3 of 3)



IDENT	LOCATION
2606	B5, A7, C9, D9
8095	B3, A5, E7, A9
7400	A1, C1, D1
7402	G1, C3, E3, F9
7404	B1, G9
7410	E1
7474	E5, E9
74123	D3, F3, G3, F7

IDENT	LOCATION
74161	C5, F5, B7, C7, D7, G7
74164	F1
74165	B9

IDENT	VALUE
R1, R4	5.1K, 1/8W, 2% Tol.
C1	NOT USED
R2, R6, R7	27K, 1/8W, 5% Tol.
C2	5-30pf Variable, E.F. JOHNSON # 275-0430-005
R3	20K, 1/8W, 5% Tol.
C3	130pf, 10% Tol., CENTRALAB # DD-131
R5	5.6K, 1/8W, 5% Tol.
C4, C5	150pf, 10% Tol, CENTRALAB # DD-151

Figure 5-30. Host Interface Board, Parts Layout Diagram and Parts List

5.2.9.1 Output Packet Buffer

The Output Packet Buffer, Figure 5-29, sheet 1, accepts serial binary data in eight-bit bytes from the PDP-11/40 Host Processor. These eight-bit bytes are stored in the buffer until a full packet of 256 bytes have been received. When the full packet is in the buffer, the Buffers Status Register shown in Figure 5-29, sheet 3, is updated in accordance with the rules listed there. When the CIE reads the Buffers Status Register (BSR), via the BEX 0 command, and finds the Output Packet Buffer full, it initiates (via the DEV 1=2 instruction) the transfer of the packet from the buffer to the CIE data memory (Output Queue). This transfer is accomplished in a bit-parallel, byte-serial mode at a rate of approximately 1.25 Megabytes per second. When the entire packet has been transferred, the BSR is again updated (LSB cleared, per Figure 5-29, sheet 3).

Hence, the Output Packet Buffer performs two functions: (1) Receives data from the PDP-11/40, and (2) transfers that data to the Host CIE Output Queue. The first function is under control of the Host Processor and is initiated in response to an "Output Buffer Empty" condition. This condition is signalled to the Host processor via the BEX 2, A2=A2 instruction, as executed by the Host CIE. The second function is under control of the Host CIE and is initiated in response to an "Output Buffer Full" condition. This condition is signalled to the CIE when it reads the Buffer Status Register. Refer to Figure 5-29, sheet 3. The Status Register is read via the BEX 0 instruction, as executed by the Host CIE.

5.2.9.1.1 Receiving Data From the Host Processor PDP-11/40

Refer to Figure 5-29, sheet 1. The serial binary data from the PDP-11/40 enters the Buffer Input Register (BIR) via terminal 2R. The gates between 2R and the BIR provide buffering and isolation to permit use of the data signal for other purposes (see paragraph 5.2.9.4). The BIR provides serial-to-parallel conversion of each 8-bit byte. The parallel outputs are applied to the Buffer Memory (BM1 and BM2) via the Buffer Input Switches (BIS-1 and BIS-2). These switches provide a direct path for the data during input to the Buffer Memory, but effectively open this input path (via the high impedance of tri-state logic) during the time that output is transferred from the Buffer Memory to the CIE Data Memory. The switches are controlled by the DEV 1=2 command and the resulting DEV 1=2 signal of the CIE.

Data from the PDP-11/40 is strobed into the BIR via a 560 KHz clock, which is also received from the PDP-11/40. This same clock serves as the input to the Bit Counter (BC). When the BC reaches a count of eight (eight bits in the BIR), it triggers the one shot (D3-5) which, in turn, generates a write pulse to the Buffer Memory (BM1 and BM2). This write pulse strobes the data bits from the BIR into the Buffer Memory. The output of another one shot (D3-13) clears the BC so that it may begin counting the next eight bits. In addition, this one shot output increments the Buffer Address Register (BAR-1 and BAR-2) so that the next byte will be stored in the next Buffer Memory location.

The Buffer Memory consists of two memory chips, each consisting of 256 locations, with four bits per location, or address. Thus, BM2 stores the four most significant bits, and BM1 the four least significant bits, of each byte. Together, they store a complete packet, or 256 bytes. The memory chips are always in the read mode, except during the pulse time (approximately 400 nsecs) of the write pulse. The write pulse can be applied to BM1 and BM2 only while DEV 1=2 is low. In effect,

data may be received from the PDP-11/40 only while the DEV 1=2 condition is not active.

When a full packet of 256 bytes has been received, the BAR's will have reached a combined count of 255, and the carry outs (CO's) will both be high. The CO's are NANDed and used to trigger the one shot (F3-5 on Figure 5-29, sheet 3) which, in turn, sets the LSB of the Status Register.

With the LSB of Status Register (SR) set, the packet is ready to be transferred from the Output Packet Buffer to the CIE Output Queue. To determine that the LSB is set, the contents of the SR are periodically read into the CIE via the BEX 0 instruction and tested by the IF LST instruction.

5.2.9.1.2 Transferring Data to the CIE Output Queue

Transfer of data from the Output Buffer to the Host CIE Output Queue is initiated when the CIE executes the DEV 1=2 instruction. This results in the DEV 1=2 signal going high. Refer to Figure 5-29, sheet 1. DEV 1=2 going high causes the Buffer Input Switches to assume the high impedance (effectively open) state. As a result, the outputs of the Buffer Memory (BM1 and BM2) are applied to the inputs of the CIE Data Memory via the CIE Ancillary Board.

The DEV 1-2 signal is inverted and applied to the NAND gate (C1-2) as a low, holding the Read/Write (R/W) input of the Buffer Memory in the read state (high). The inverted DEV 1=2 signal is also applied to the NOR gate to enable the Incrementing signal to the clock input of the BAR's. Finally, the rising edge of the DEV 1=2 signal triggers a one shot (D3-13) which, in turn, clears the BAR's to zero. It should be noted that the DEV 1=2 signal remains high during the transfer of the packet to the CIE Output Queue, and goes low only when the next DEV 1 Instruction is exectued.

With the BAR's cleared to zero, a zero address is applied to the BM and the data at location zero appears on the BM data output lines. These lines are connected to the CIE Output Queue data input lines via the CIE Ancillary Board. Appropriate Memory Address Register and write pulse operation on the CIE Ancillary Board causes this data to be written into the CIE Output Queue.

While DEV 1=2 is high, an increment pulse will be generated on the CIE Ancillary Board for each CIE instruction cycle. This increment pulse will increment the Memory Address Register on the CIE Ancillary Board, and will also be applied to the BAR's on the Host Interface Board. This signal is routed through two NOR gates to the clock input of the BAR's. The first NOR (C3-10) will inhibit the increment input when DEV 1=2 is not active. The second NOR (F9-10) permits an alternate clock input to the BAR's when DEV 1=2 is not active, i.e., when data is being fed into the Buffer from the Host Processor.

The BARs are incremented by one count for each increment pulse applied. These incremented addresses are, in turn, applied to the BM. Hence, the data at each word location of the BM is read out in sequence to the CIE Output Queue. When the count reaches 255, the entire packet has been transferred and the increment pulses are terminated via the CIE Ancillary Board. Also, a count of 255 in the BAR's provides an output in the form of the Combined Carry Out to one shot F3 on Figure 5-29, sheet 3. This one shot pulses the clear input of the SR LSB. This action clears

the LSB and indicates that the Output Buffer is empty. This condition will be determined by the CIE upon the next execution of a BEX 0 Instruction. Also, the Output Buffer Empty status will be transferred to the Host Processor upon the next execution of the BEX 2, A2=A2 Instruction.

5.2.9.2 Input Packet Buffer

The Input Packet Buffer shown in Figure 5-29, sheet 2, accepts parallel binary data (eight-bit bytes) in byte-serial form from the CIE Output Queue at a rate of approximately 1.25 Megabytes per second. These eight-bit bytes are stored in the Buffer until a full packet of 256 bytes have been received. When the full packet is in the Buffer, the BSR (Figure 5-29, sheet 3) is updated, i.e., the Most Significant Bit (MSB) is cleared. This status is transferred to the Host Processor as a result of the CIE performing the DEV 2=1 instruction. When the Host receives this status, it will begin requesting data from the Input Buffer on a word-at-a-time basis. In response to each request (the SNW signal, shown on Figure 5-29, sheet 2) from the Host, two bytes (a 16-bit word) are transferred to the Host Processor. When the last two bytes (16-bit word) of the packet are transmitted, the BSR is again updated, i.e., the MSB is set signifying Input Buffer Empty. Therefore, the next BEX 0 instruction performed by the CIE will read the BSR resulting in a determination, via an IF MSB instruction, that the Input Buffer is empty.

Thus, the Input Buffer performs two functions: (1) Receives data from the CIE's Input Queue, and (2) transfers that data to the Host Processor. The first function is under control of the Host CIE and is initiated in response to an Input Buffer Empty condition. This condition is signalled to the CIE when it reads the Buffer Status Register. See Figure 5-29, sheet 3. The Status register is read via the BEX 0 instruction as executed by the Host CIE. The second function is under control of the Host Processor and is initiated in response to an Input Buffer Full condition. This condition is signalled to the Host Processor via the DEV 2=1 instruction as executed by the Host CIE.

5.2.9.2.1 Receiving Data From the CIE Input Queue

Data from the CIE Input Queue can be transferred to the Input Buffer if the Input Buffer is empty. This condition is determined by the Host CIE via a BEX 0 command followed by an IF MST command.

Actual data transfer is initiated by the Host CIE's execution of the DEV 1=4 instruction and the resulting DEV 1=4 signal going high. Refer to Figure 5-29, sheet 2. The DEV 1=4 signal is inverted and applied to the Buffer Input Switches causing them to assume the normal (effectively closed) state. As a result, the data lines from the CIE Data Memory (Input Queue) are applied directly to the inputs of the Buffer Memory (BM1 and BM2). The inverted DEV 1=4 signal is also applied to one input of a NOR gate (G1-9) thereby enabling the increment signal to the clock input of the BAR's. In addition, this signal is applied to a NAND gate (E1-11) on Figure 5-29, sheet 3, thus enabling a clear input to the SR MSB. The DEV 1=4, prior to inversion, is applied to a NAND gate (A1-2) thus enabling a write pulse input to the Read/Write (R/W) control of the Buffer Memory. Finally, the rising edge of the DEV 1=4 signal triggers a one shot (G3-5) which, in turn, clears the BAR's to zero. It should be noted that the DEV 1=4 signal remains high during the entire time that the packet is being transferred to the buffer from the CIE Input Queue. The signal goes low again when the next DEV 1 instruction is executed.

With the BAR's cleared to zero, a zero address is applied to the BM and the data on the lines from the CIE Input Queue (via the CIE Ancillary Board) are applied to location zero of the BM. Appropriate Memory Address Register operation on the CIE Ancillary Board causes data to be read out of the CIE Input Queue.

While DEV 1=4 is high, a write pulse followed by an increment pulse will be generated on the CIE Ancillary Board for each CIE processor Instruction cycle. This write pulse is applied to the Host Interface Board and will strobe the data into the Buffer Memory. The increment pulse increments the Memory Address Register on the CIE Ancillary Board and is also fed to the BAR's (via G1-10) on the Host Interface Board, thus incrementing them. These incremented addresses are, in turn, applied to the BM. Hence, data is written into each location of the BM as it is read out of the CIE Input Queue. When the count reaches 255, the entire packet has been transferred and the CIE Ancillary Board inhibits further counting. A count of 255 in the BAR's provides an output in the form of the Combined Carry Outs at B1-2 to the one shot (F7) on Figure 5-29, sheet 3. This one shot, in turn, pulses the clear input of the SR MSB. Therefore, the MSB is cleared, indicating that the Input Buffer is full. This condition will be determined by the CIE upon the next execution of a BEX 0 instruction. Also, this status will be transferred to the Host Processor upon the next execution of a DEV 2=1 Instruction.

5.2.9.2.2 Transferring Data to the Host Processor PDP-11/40

Transfer of the 256-byte packet of data from the Input Buffer to the Host Processor can be accomplished only when the DEV 1=4 signal is low. Refer to Figure 5-29, sheet 2. In this condition, the R/W input of the BM is held high (read state for BM), the increment input to the BAR's is inhibited, a BAR's clock input from the Bit Counter (BC) is enabled, the Buffer Input Switches (BIS's) are effectively opened, and a NAND gate, shown on Figure 5-29, sheet 3, is enabled to permit setting the MSB of the SR.

Transfer of data from the Input Buffer to the Host Processor is actually initiated by the execution of the DEV 2=1 instruction by the Host CIE. The DEV 2'=1 signal (Figure 5-29, sheet 2) goes low for one instruction time, and clears the BAR's to zero when gated with the signal at 2Y. It also triggers the BOR One Shot (G3, pin 2) which, in turn, provides a load pulse to the Buffer Output Register (BOR). Note that the load pulse to the BOR must be greater than 900 nsecs but less than 1200 nsecs.) Hence, the contents (eight bits) of location zero of the Buffer Memory are loaded into the BOR and are ready for transmission in serial form to the Host Processor.

In addition to zeroing the BAR's and loading the first word into the BOR, the DEV 2'=1 signal transfers the status (contents) of the BSR to the Host Processor. In this case, the status is Input Buffer Full. This status signal is transmitted as a positive pulse from the Status Output Gate (F9, pin 13) and is one instruction period long or approximately 1 µsec. The output pulse is apparent at pin 1S. Refer to Figure 5-29, sheet 3.

When the Host Processor is aware of the Input Buffer Full status, it requests a word-at-a-time from the Input Buffer by sending a Send Next Word (SNW) signal for each 16-bit word requested. The SNW signal is received at terminal 1I of the Host Interface Board. Refer to Figure 5-29, sheet 2. This signal is a negative

pulse greater than 1.8 μsecs (ideally 2.2 μsecs). This pulse is clocked into a flip-flop to minimize false inputs and to synchronize the start of data output. The flip-flop output triggers the one-shot which, in turn, clears the Bit Counter (G7) and the Control Flip-Flop (E5). The output of the Control Flip-Flop goes high, enabling the 560 KHz clock input (CKO). This clock then drives the Bit Counter (G7) and the BOR, each clock (positive edge) shifting a data bit (at 2G) to the Host Processor. This clock is also an output at 1F to the Host Processor. With the eighth clock pulse, the first byte is completely clocked out of the BOR and the Count 8 output from the BC goes high. The Count 8 output then increments the BAR's, thereby allowing the next word of the BM to appear at the BOR inputs. The Count 8 output also triggers the BOR one shot which generates the load pulse to load the next byte into the BOR. The next eight clock pulses (pulses 9 through 16) clock out the second byte to the Host Processor. The sixteenth clock pulse causes the Count 16 signal to the Control Flip-Flop to go high. The rising clock edge occurs during a high on the flip-flop's data input, resulting in a low output from the flip-flop. This inhibits further clock (CKO) inputs to the BC and the BOR. The CKO clock will not be re-enabled until the next SNW pulse is received. At that time the next 16-bit word (two eight-bit bytes) will be sent to the Host Processor. When the entire packet of 256 bytes has been shifted out, the BAR's will have reached a combined count of 255 and the Combined Carry Out (CCO) will go low. The CCO is inverted and triggers one shot F7 on Figure 5-29, sheet 3. The one shot sets the SR MSB indicating that the Input Buffer is empty. Hence, the next time the Host CIE executes a BEX 0 instruction, it will find the Input Status Register empty.

5.2.9.3 Buffers Status Register

The Buffers Status Register (BSR) is a two-bit register consisting of two flip-flops. Refer to Figure 5-29, sheet 3. The LSB stores the status of the Output Buffer and the MSB stores the status of the Input Buffer. The LSB is either cleared by the combination of DEV 1=2 and COOB or set by the combination of DEV 1=2' and COOB. The MSB is either cleared by the combination of DEV 1=4 and COIB or set by the combination of DEV 1=4' and COIB. Note that both COIB and COOB must always be greater than 1 microsecond; ideally 1.5 μsec.

Setting both LSB and MSB is inhibited while the BEX 0' signal is low, the low occurring during the time that the contents of the BSR is being read by the Host CIE via the BEX 0 command. When the BSR is read into the CIE's B register, via the BEX 0 command, the content of LSB appears in the Least Significant Bit as well as all odd numbered bits of the B register. The content of MSB appears in the most significant bit as well as all even numbered bits of the B register. During the BEX 0 instruction, which involves eight clock pulses, the contents of the BSR are shifted circularly so that they end up in their original locations.

The content of the BSR is transferred to the Host Processor as a result of the Host CIE's executing the BEX 2, A2=A2 command and/or the DEV 2=1 command. That is, the BEX 2' and the DEV 2' signals go low and gate the status to pins 1H and 1S. Refer to Figure 5-29, sheet 3. The resulting pulses are one instruction period long (approximately 1 μsec).

5.2.9.4 Interface With Loader Boards

The data and clock inputs at 2R and 1T, shown in Figure 5-29, sheet 1, are buffered and routed to the Loader boards of all three ESM cabinets. That is, the data signals as received from the Host Processor are forwarded to the three Loader boards via the outputs at 1W, 1U, and 1V for cabinets 1, 2, and 3, respectively. The associated clock signals are forwarded to the three Loader boards via the outputs at 1Y, 1R, and 1X for cabinets 1, 2, and 3, respectively.

5.2.10 UNIVERSAL INTERFACE BOARD

The Universal Interface Board consists of an M1710 UNIBUS Interface Foundation Module (as manufactured by Digital Equipment Corporation) together with the custom logic which has been added to the board to make it compatible with ESM. See Figures 5-31 and 5-32. This board is installed in the PDP-11/40 Processor and interfaces on one side to the UNIBUS of the PDP-11/40, and on the other side to the ESM. The interface to the ESM is in the form of serial binary transmission at a rate of 560 kbps and employs TTL signal levels. Transmission is in the form of one word (16 bits) at a time in half-duplex mode (one direction at a given time). The complementing interface board at the ESM end is the Host Interface Board, described in paragraph 5.2.9 of this manual. The Universal Interface Board in the PDP-11/40 is interconnected with the Host Interface Board in the ESM cabinet by a 100 foot (maximum) cable, described in section 5.4 of this manual.

The M1710 UNIBUS Interface Foundation Module, as provided by Digital Equipment Corporation, is documented in:

1. The Module Data Sheet, dated April 1974 and entitled, "M1710 UNIBUS Interface Foundation Module."

2. The module logic diagram; parts layout and parts list, consisting of four sheets, dated June 1973.

Both of these documents are provided with the module, by Digital Equipment Corporation.

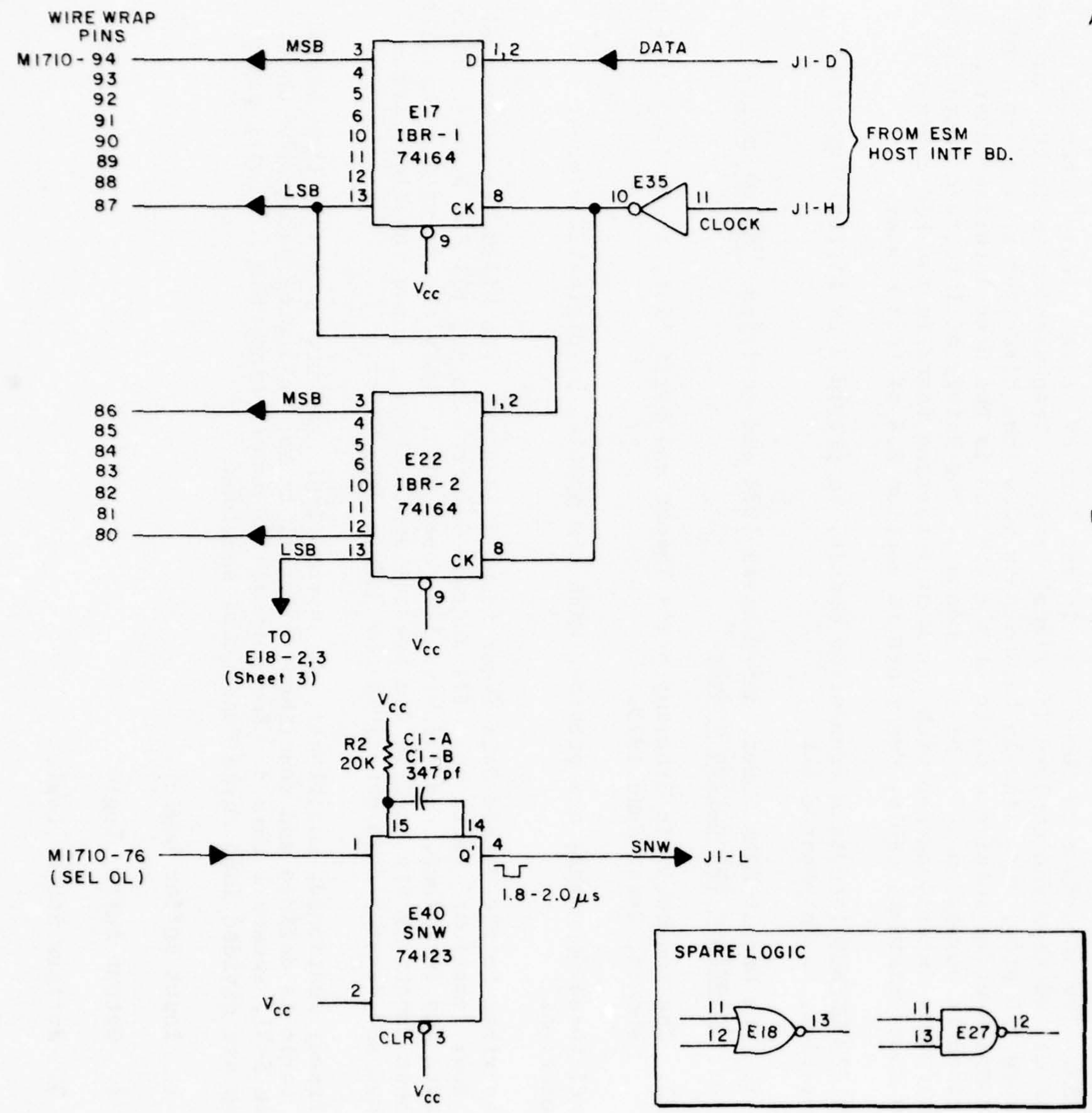
As described in the Module Data Sheet identified above, the M1710 can be divided into four functional sections: (1) Address Selector Logic, (2) Bus Request Logic, (3) Data Bus Interface, and (4) Miscellaneous Logic. Only the first and the third of these functions are used in the present application. These functions are defined and described in detail in the Module Data Sheet.

As already mentioned, additional, or custom, logic has been added to this board. This logic is defined and described in detail in the following paragraphs and in Figure 5-31, sheets 1 thru 3. For purposes of description, the following paragraphs are divided into three functional sections:

1. Input Buffer Logic

2. Output Buffer Logic

3. Buffers Status Logic



ADD WIRE WRAPS ON M1710 Bd FOR OPTIONS

FROM	TO	
M1710- 9	M1710- 1	ADDRESS SELECT
11	2	
13	3	
16	4	
17	5	
19	6	
21	7	
23	8	
GND	36 DECODER ENBL	

INSTALL CABLE CONN. GND STRAPPING ON
M1710 Bd

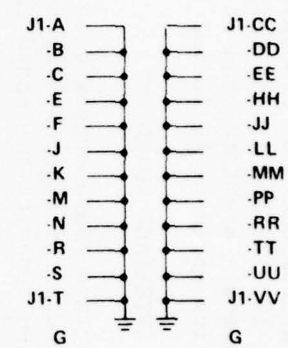


Figure 5-31. Universal Interface Board Logic (Sheet 1 of 3)

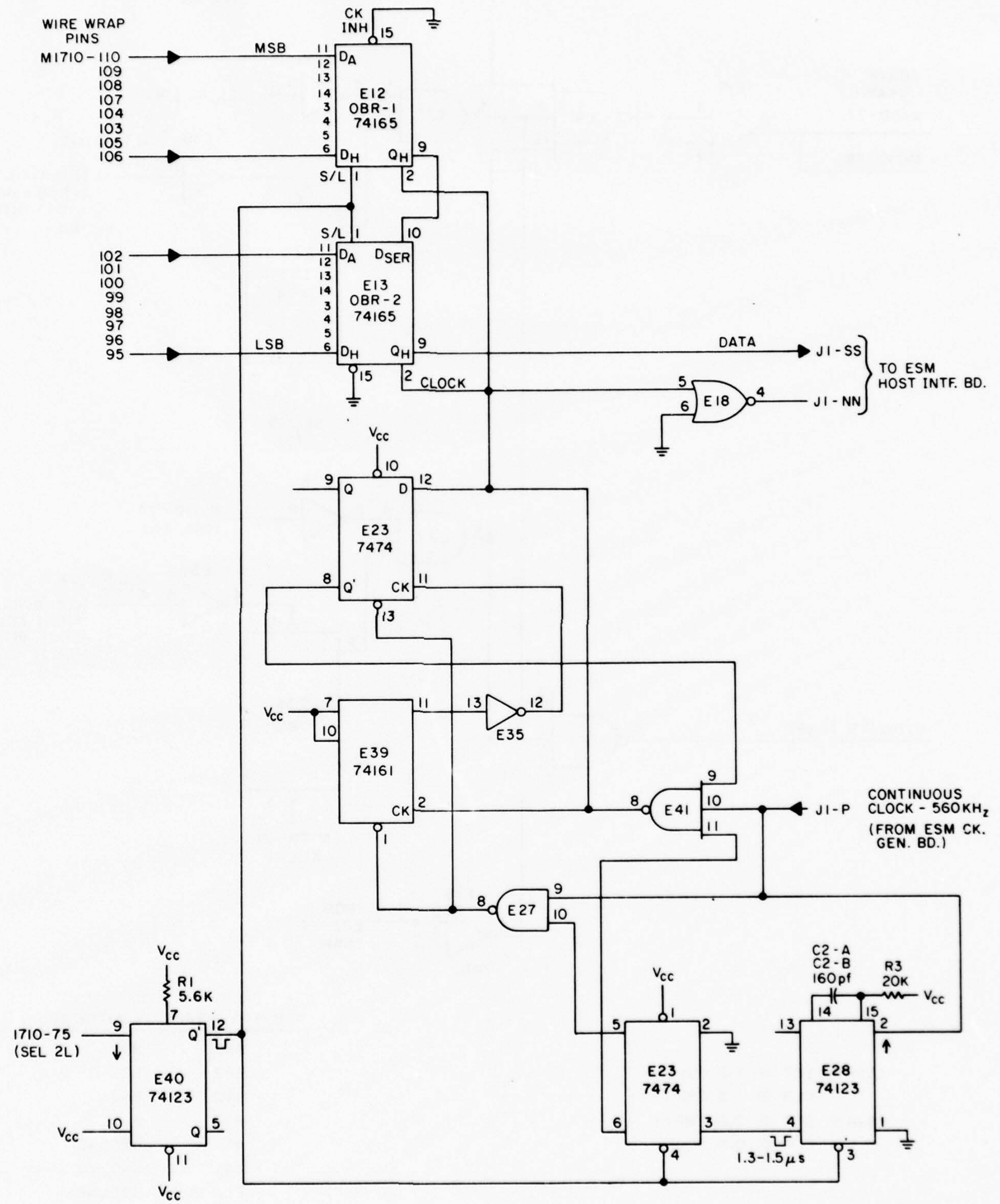
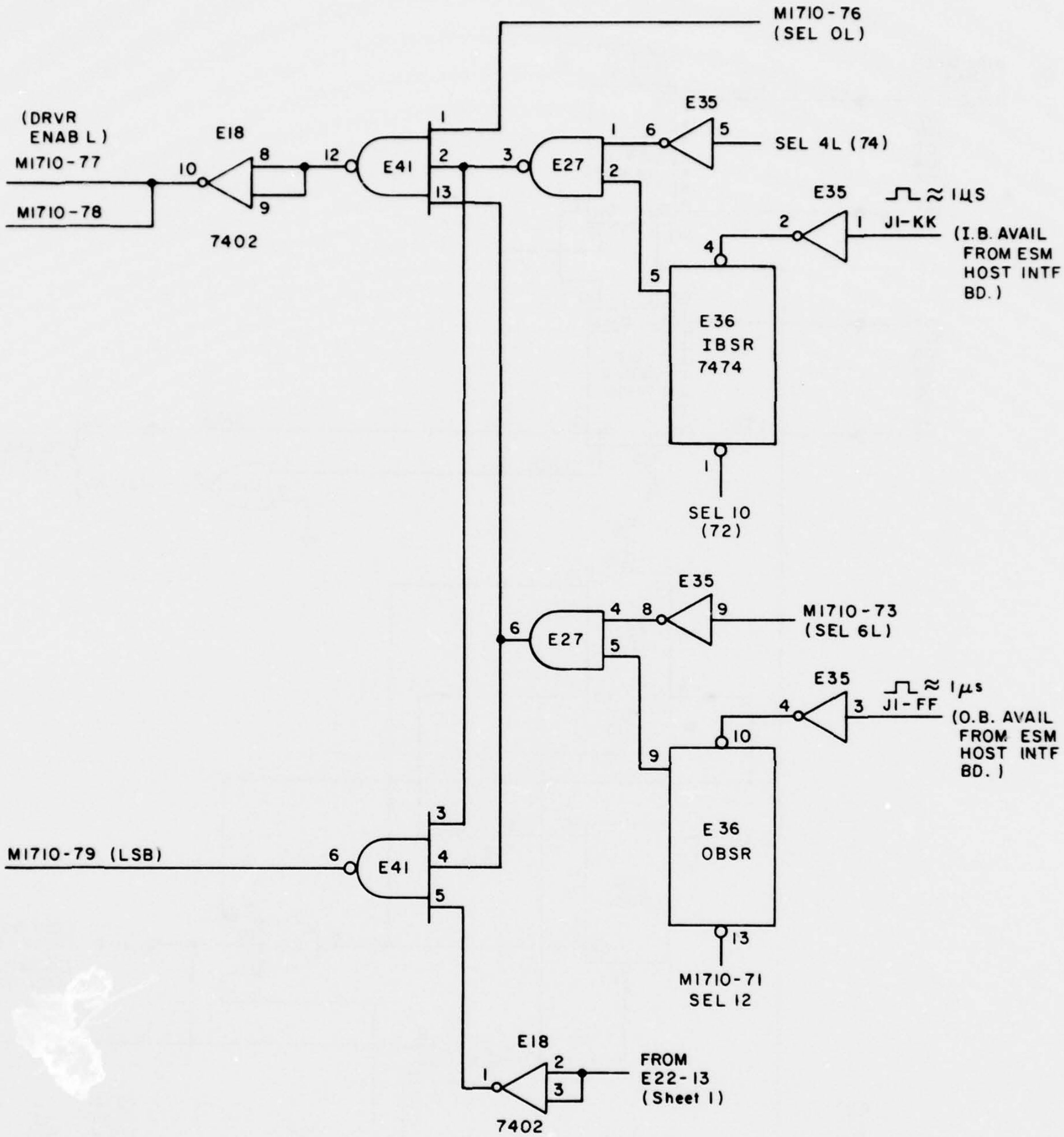


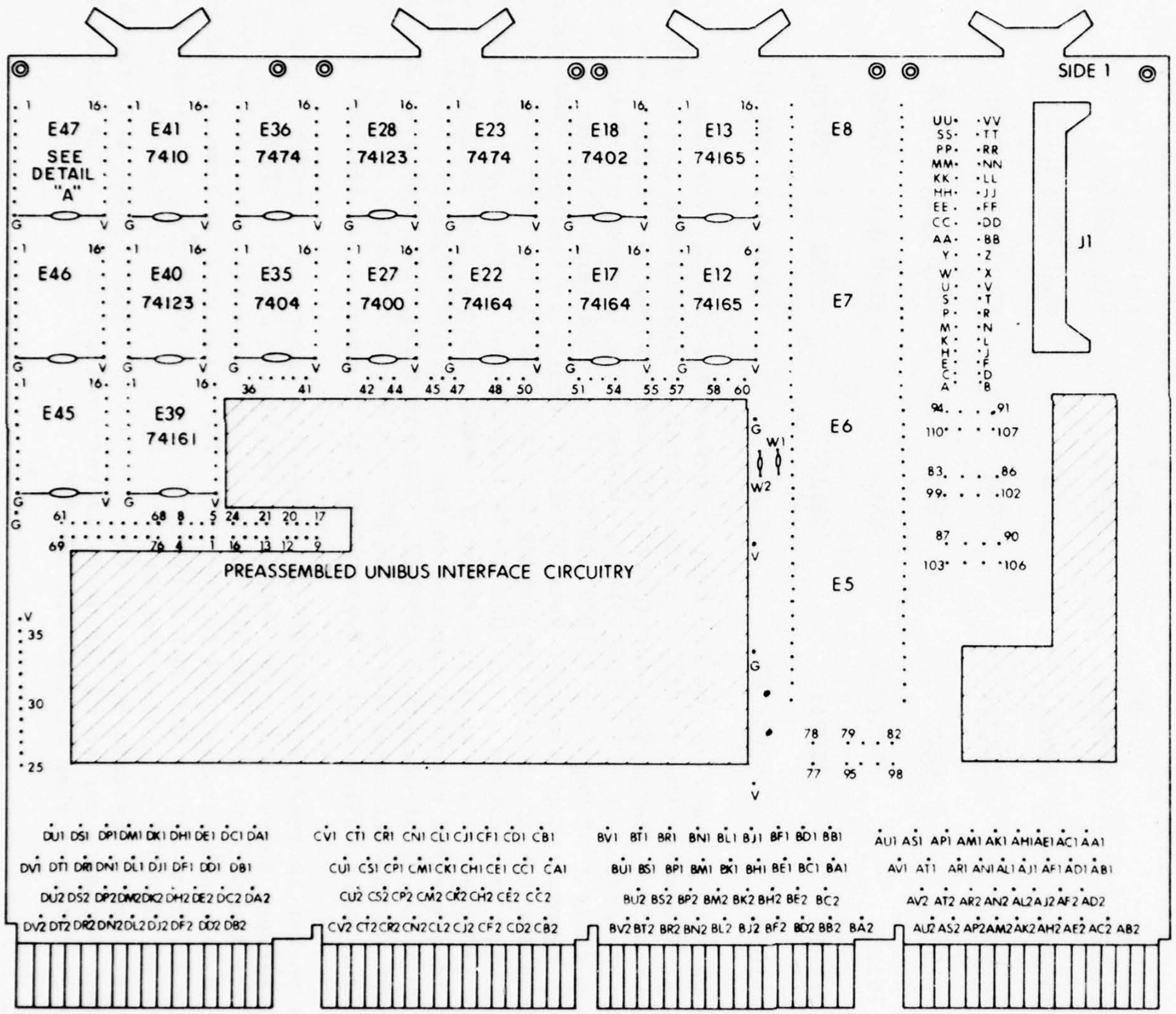
Figure 5-31. Universal Interface Board Logic (Sheet 2 of 3)



ADD WIRE WRAPS ON M1710 BD		
BS2	-	BT2
BP2	-	BR2
BM2	-	BN2
BK2	-	BL2
43	-	GROUND
44	-	GROUND
E21-13	-	GROUND

IBSR ≡ SET ≡ I.B. FULL
CLR ≡ I.B. EMPTY
OBSR ≡ SET ≡ O.B. EMPTY
CLR ≡ O.B. FULL

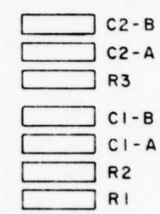
Figure 5-31. Universal Interface Board Logic (Sheet 3 of 3)



7400	E27
7402	E18
7404	E35
7410	E41
7474	E23, E36
74123	E28, E40
74161	E39
74164	E17, E22
74165	E12, E13
R1	5.6K, 1/8 W, 5% TOL.
R2,R3	20K, 1/8 W, 5% TOL.
C1-A	300 Pf, 10% TOL., DD-301*
C1-B	47 Pf, 10% TOL., DD-470*
C2-A	150 Pf, 10% TOL., DD-151*
C2-B	10 Pf, 10% TOL., DD-100*

*CENTRALAB PART NO. IS LISTED.
C1-A IS WIRED IN PARALLEL WITH C1-B
C2-A IS WIRED IN PARALLEL WITH C2-B

DETAIL "A"



•= WIREWRAP PIN
G= GROUND
V= +5V
E = IC NUMBER

Figure 5-32. Universal Interface Board, Parts Layout Diagram and Parts List

These sections of the custom logic are described in detail after the following general operational description of the overall board.

5.2.10.1 General Operational Description

The Universal Interface Board (M1710 plus added custom logic) consists of the equivalent of six registers which interface with the PDP-11/40 UNIBUS. Each of these registers is addressed via a unique address similar to any other register or memory location having access to the UNIBUS. Each of these registers, in turn, is associated with an array element in the user program. In addition, each of these registers has associated with it, a signal name in the M1710 logic. This signal interfaces with the custom logic added to the board. The parameters of these six registers are tabulated below:

Register Address	Array Element	Signal Name	Functional Description
761000	DEVST(1)	SEL0	READ DATA WORD
761002	DEVST(2)	SEL2	WRITE DATA WORD
761004	DEVST(3)	SEL4	READ I.B. STATUS
761006	DEVST(4)	SEL6	READ O.B. STATUS
761010	DEVST(5)	SEL10	CLEAR I.B. STATUS
761012	DEVST(6)	SEL12	CLEAR O.B. STATUS

When a packet is ready at the ESM Host Interface Board (HIB) for transfer to the UNIVERSAL Interface Board (UIB) a status signal is transmitted to the UIB, setting the Input Buffer Status Register (IBSR), Address 761004, on the UIB. When the content of address 761004 (DEVST(3)) is subsequently examined and found to be odd, the content of register 761000 (DEVST(1)) is transferred to the input data array in memory. Each transfer from DEVST(1) results in a signal (SNW) being sent back from the UIB to the HIB requesting the transfer on the next word (16 bits). As each word is received at the UIB it is transferred to the input data array in memory. A total of 129 such transfers are made; however, the first word transferred is discarded since it represents the contents of register 761000 prior to receipt of the first word from the HIB. The remaining 128 words (16 bits each) represent the packet received from the ESM via the HIB. After receipt of the full packet the Input Buffer Status Register (IBSR) is cleared via DEVST(5) = 0.

When a packet is ready at the PDP-11/40 Host Processor for transfer to the ESM Host Interface Board (HIB), the Output Buffer Status Register (DEVST(4)) is examined. If found to be odd, the HIB buffer is empty and ready to receive data. Hence, data can be transmitted to the HIB. The first word is transferred from the data array in memory to the Output Buffer Register (DEVST(2)). As soon as it is present in DEVST(2) it is clocked out serially to the HIB in the ESM. The remaining 127 locations in the data array are fed out in this same fashion and transferred to the HIB. Hence, a packet of 128 words is received at the HIB. The Output Buffer Status Register is then cleared via DEVST(6) = 0.

5.2.10.2 Input Buffer Logic

The Input (with respect to the PDP-11/40) Buffer Logic (Figure 5-31, sheet 1) allows serial data bits and accompanying clock to be received at pins J1-D and J1-H, respectively, from the HIB. The data is received at 560 kbps in groups of 16 bits (one word for the PDP-11/40). Each 16-bit word is stored in IBR-1 and IBR-2 (DEVST(1)) until it is transferred to data memory. Moving DEVST(1) to memory results in the SEL 0L signal (at pin M1710-76) going low. This causes an output pulse from E40 to be transmitted from pin J1-L to the HIB. This Send Next Word (SNW) signal causes the next 16-bit word to be transmitted from the HIB to IBR-1 and IBR-2.

The outputs of IBR-1 and IBR-2 interface with the UNIBUS drivers on the M1710 Board. Those interface connections are at wire-wrap pins 94 through 79. Note that pin 79 appears on Figure 5-31, sheet 3. Normally data enters pin 79 via pin 5 of E41 (Figure 5-31, sheet 3). Pins 3 and 4 of E41 are normally high as a result of the signals SEL 4L and SEL 6L being high at the time SEL 0L goes low. Note that only one of these signals can be low at a given time. Also note that when SEL 0L goes low, the signal labeled DRVR ENAB L goes low at pins 77 and 78 (Figure 5-31, sheet 3) of the M1710 Board. This signal enables the UNIBUS Drivers on the M1710 Board, thereby allowing data to be applied to the data lines of the UNIBUS.

The output of the one shot on Figure 5-31, sheet 1, must have a duration of at least 1.8 microseconds for proper operation with the HIB.

5.2.10.3 Output Buffer Logic

The Output (with respect to the PDP-11/40) Buffer Logic (Figure 5-31, sheet 2) allows a 16-bit word, as received from the UNIBUS, to be transferred in serial form to the HIB. The outputs of the UNIBUS receivers on the M1710 Board appear at wire-wrap pins 110 through 95, and serve as inputs to the Output Buffer Register OBR-1 and OBR-2 (DEVST(2)). When a word is transferred from the PDP-11/40's memory to the Output Buffer Register, the signal line SEL 2L goes low causing an output from the one shot E40. This output is used as the load pulse for OBR-1 and OBR-2 , clears the one shot E28, and presets the first flip-flop of E23.

Clock (560-KHz square wave) is continuously being received at pin J1-P from the HIB, and is applied to the one shot E28 and NAND gates E27 and E41. As a result, the one shot is continually triggered, the first flip-flop of E23 continually provides a low to pin 10 of NAND gate E27, the counter E39 counts up and provides a carry-out to the second flip-flop of E23. A low output from this flip-flop is provided to the NAND gate E41 thereby inhibiting clock to the counter E39 and to the Output Buffer Register (OBR-1 and OBR-2).

When SEL 2L goes low, the output from E40 clears the one shot (E28) for the duration of E40's output and presets the first flip-flop of E23. The output of the flip-flop enables NAND gate E27 thereby gating a clear pulse to counter E39 and the second flip-flop of E23. Clock pulses are now enabled to the counter (E39) and to OBR-1 and OBR-2. Hence, the data previously loaded in OBR-1 and OBR-2 is clocked out at pin J1-SS and on to the HIB. Clock is also routed to the HIB via pin J1-NN. When the counter (E39) reaches a count of 16, the carry-out pulse clocks the second flip-flop of E23 thereby causing a low to be applied to NAND gate E41 and

inhibiting clock to the Output Buffer Register and to the counter. Hence, a 16-bit word has been transmitted to the HIB. The entire process is repeated each time a new word is transferred to the Output Buffer Register and signal SEL 2L goes low.

5.2.10.4 Buffer Status Logic

The Buffer Status Logic provides the capability for storing and examining the status of the buffers contained on the HIB, which is remote from the UIB. These buffers, the Input Buffer and the Output Buffer, are each capable of holding 256 bytes (i.e., 128 16-bit words). When the Input Buffer is filled on the HIB or the Output Buffer is emptied on the HIB, that status condition is reported to the Input Buffer Status Register (IBSR) and the Output Buffer Status Register (OBSR), respectively, on the UIB. This reporting is accomplished by the transmission of a pulse from the HIB to the preset inputs of IBSR and OBSR, respectively. These pulses enter the board at J1-KK and J1-FF. See Figure 5-31, sheet 3.

IBSR and OBSR correspond to addresses 761004 and 761006, respectively. Hence, the status (content) of these registers is read via DEVST(3) and DEVST(4), respectively. Referring to Figure 5-31, sheet 3, these correspond to signals SEL 4L and SEL 6L. Now, if IBSR has been preset (indicating that the Input Buffer on HIB is full) its output at pin 5 will be high. Hence, when SEL 4L goes low (contents of IBSR being read), the output at E27, pin 3, will go low. This results in lows at E41, pins 12 and 6. Pin 6 represents the least significant of the 16 data lines to the UNIBUS. Thus, as a result of the DEVST(3) and SEL 4L signal, the LSB will be determined by the contents of the IBSR; the other 15 bits will be in accordance with the content of IBR-1 and IBR-2 of Figure 5-31, sheet 1. However, only the LSB is of concern since the test to determine status is based upon the 16-bit word being either odd (Input Buffer Full) or even (Input Buffer Empty).

The content of OBSR is read and tested in the same manner as IBSR, except that DEVST(4) and the signal SEL 6L are involved. Again, the state of the LSB defines the status in that if the word is odd, the Output Buffer is empty; and, if the word is even, the Output Buffer is full.

Note that the wire-wraps tabulated in Figure 5-31, sheet 1, are required to establish the basic address selection and to provide required ground connections. Refer to the Module Data Sheet provided by Digital Equipment Corporation with the M1710 Board.

5.2.11 GATEWAY INTERFACE BOARD

A Gateway Interface Board (GIB) in one ESM Loop, together with another identical GIB in another ESM Loop, allows two loops to interface with each other and exchange data packets with each other (see Figures 5-33 and 5-34). With this configuration, ASCII characters (seven bits plus parity) are exchanged between the GIBS on a serial transmission basis, in the asynchronous mode, at 560 Kilobits per second. Each exchange involves a packet of data comprising 256 characters.

The Gateway Interface Board consists of: (1) An Output Packet Buffer, with respect to the other (remote) Loop, (2) an Input Packet Buffer with respect to the other (remote) Loop, and (3) a Buffer Status Register.

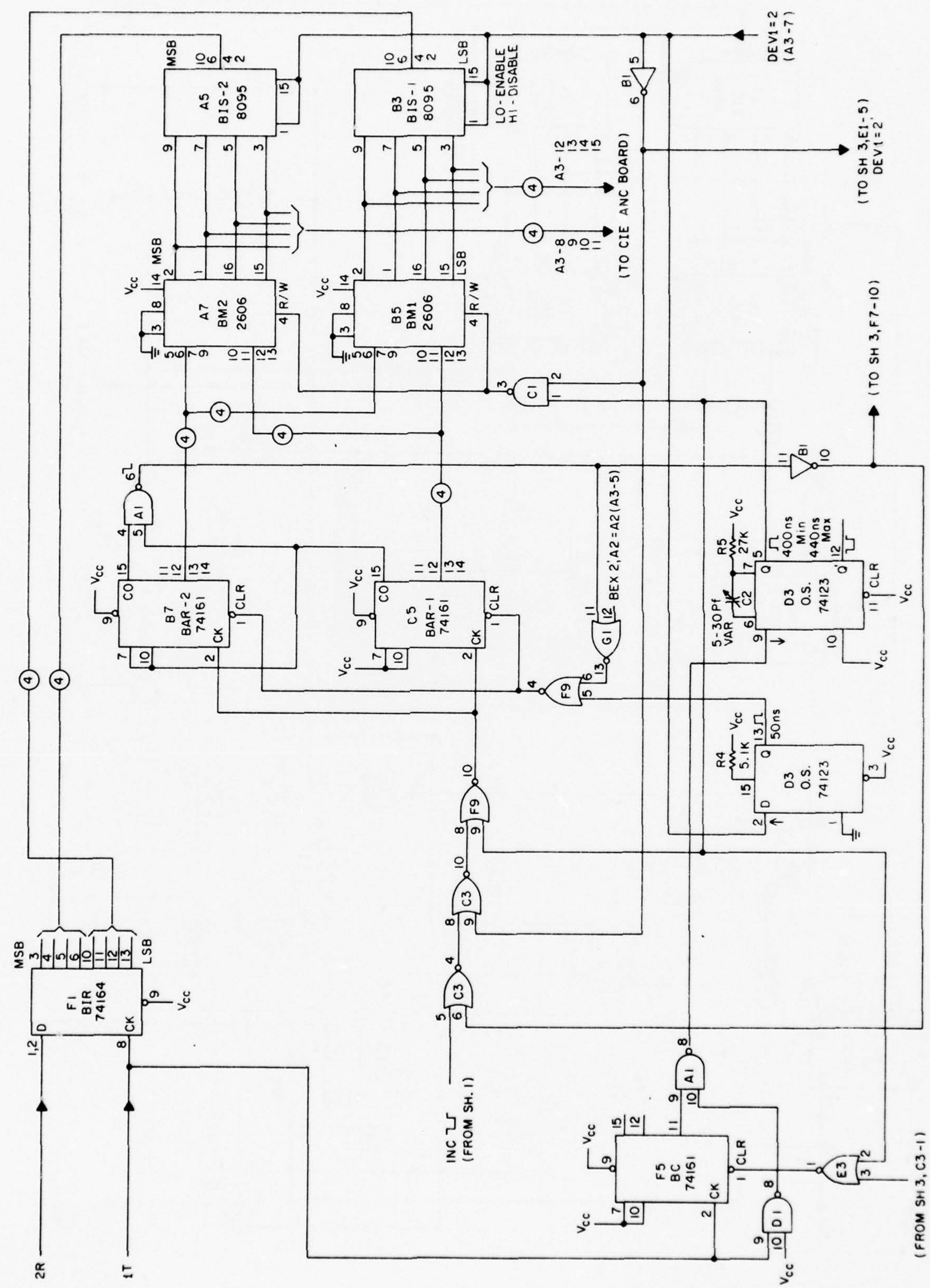


Figure 5-33. Gateway Interface Board Buffer Logic (Sheet 1 of 3)

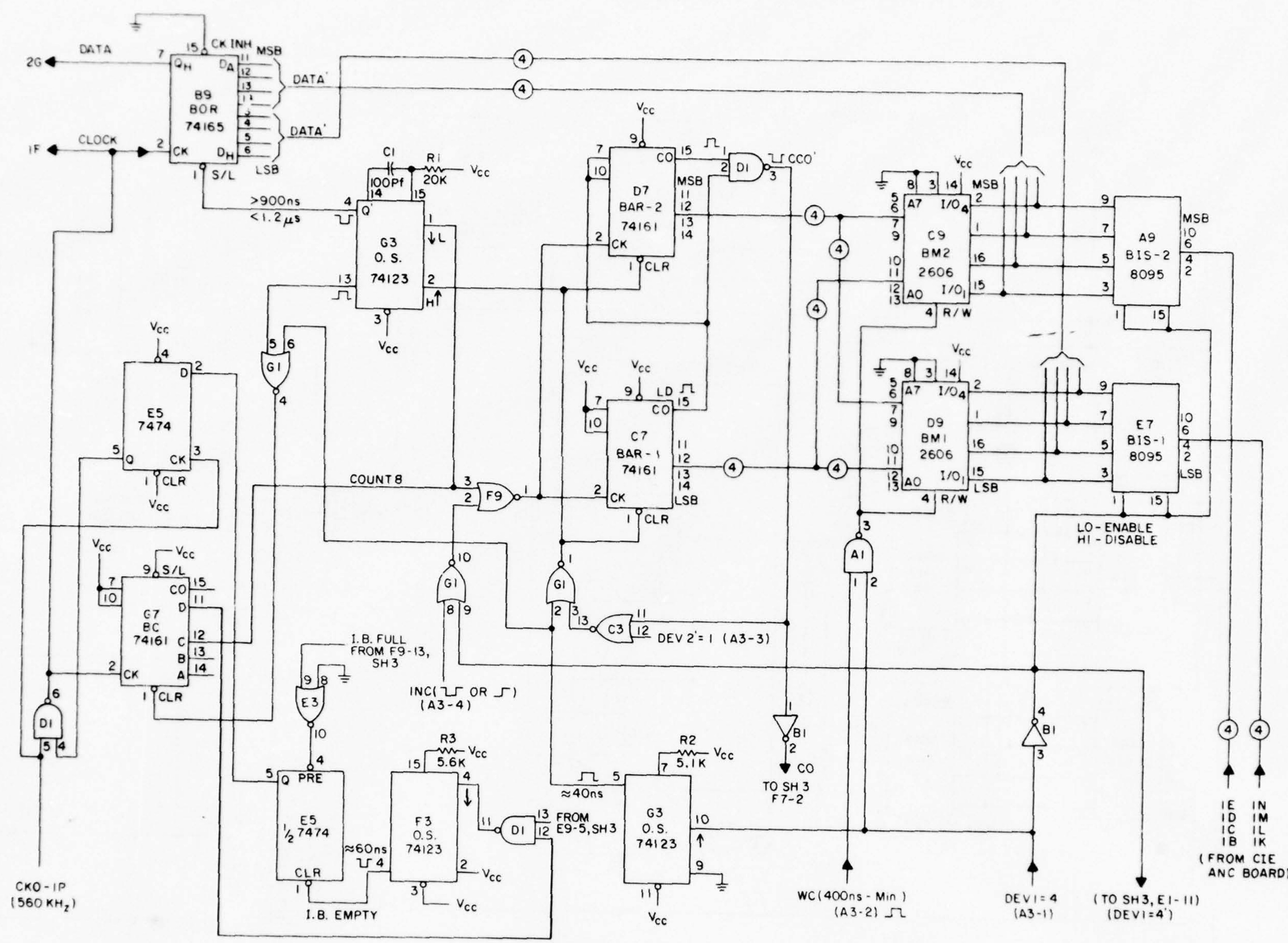


Figure 5-33. Gateway Interface Board Buffer Logic (Sheet 2 of 3)

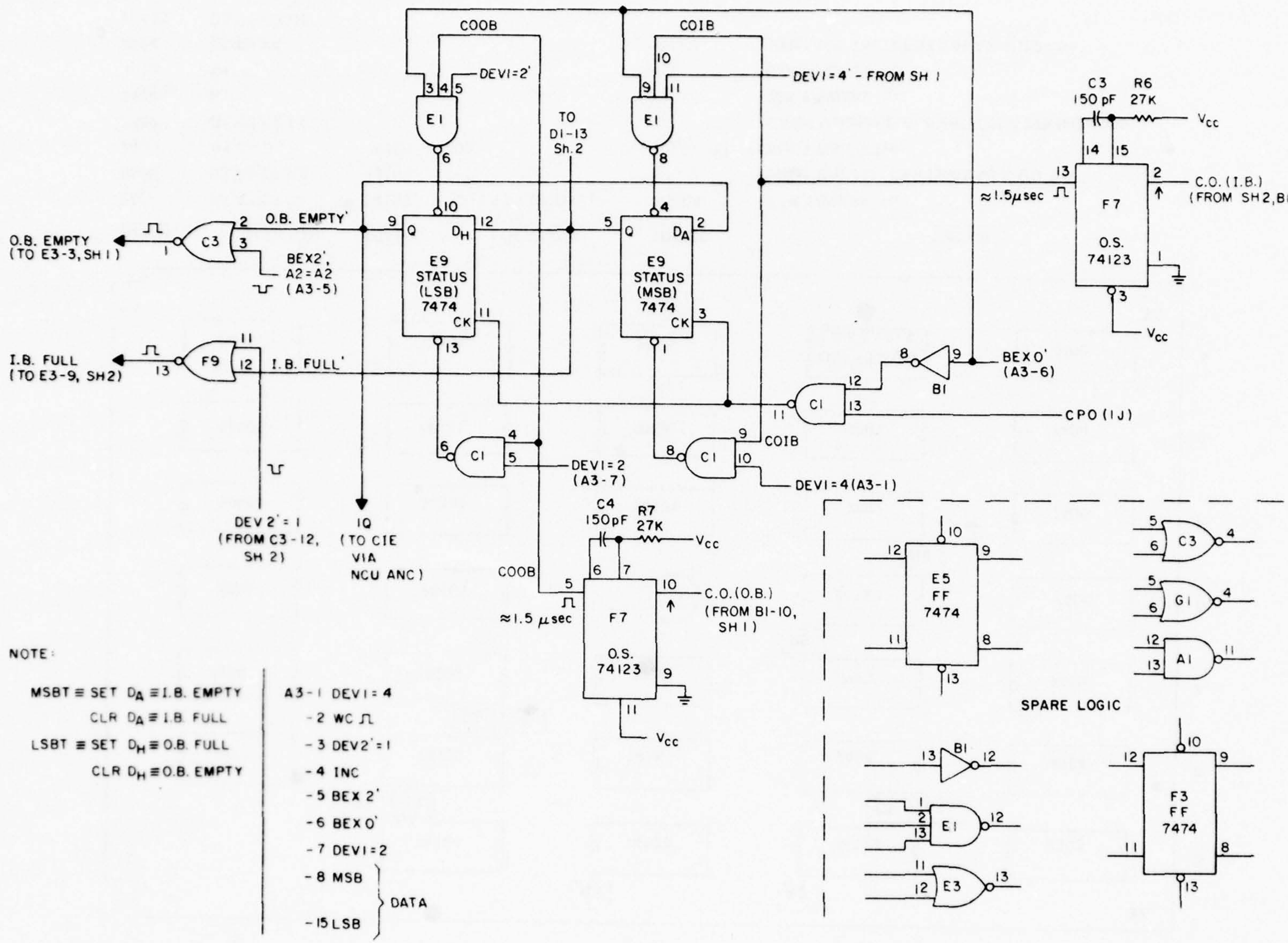
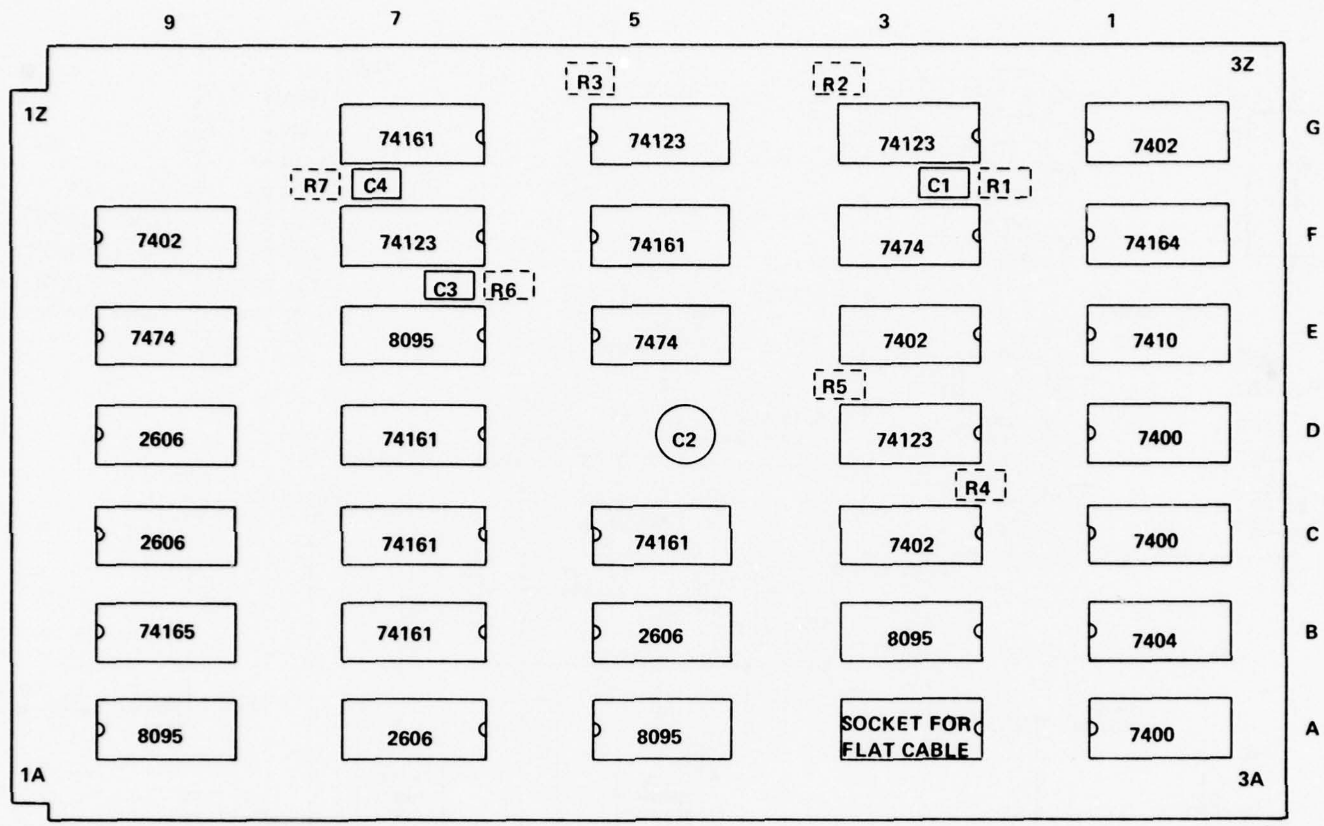


Figure 5-33. Gateway Interface Board Buffer Logic (Sheet 3 of 3)



IDENT	LOCATION	IDENT	LOCATION	IDENT	VALUE
2606	B5,A7,C9,D9	74161	C5,F5,B7,C7,D7,G7	R2,R4	5.1K,1/8W,2% Tol.
8095	B3,A5,E7,A9	74164	F1	C1	100pf,10% Tol., CENTRALAB # DD-101
7400	A1,C1,D1	74165	B9	R5,R6,R7	27K,1/8W,5% Tol.
7402	G1,C3,E3,F9			C2	5-30pf Variable,E.F. JOHNSON # 275-0430-005
7404	B1			R1	20K,1/8W,5% Tol.
7410	E1			R3	5.6K,1/8W,5% Tol.
7474	E5,E9,F3			C3,C4	150pf.10% Tol., CENTRALAB # DD-151
74123	D3,F7,G3,G5				

Figure 5-34. Gateway Interface Board, Parts Layout Diagram and Parts List

5.2.11.1 Output Packet Buffer

The Output Packet Buffer, shown in Figure 5-33, sheet 1, accepts serial binary data in eight-bit bytes, or characters. These eight-bit bytes are stored in the buffer until a full packet of 256 bytes have been received from the remote GIB. When the full packet is in the buffer, the Buffers Status Register, shown in Figure 5-33, sheet 3, is updated in accordance with the rules listed there. When the CIE reads the Buffers Status Register (BSR), via the BEX 0 command, and finds the Output Packet Buffer full, it initiates (via the DEV 1=2 instruction) the transfer of the packet from the buffer to the CIE data memory, specifically, the Output Queue. This transfer is accomplished in a bit-parallel, byte-serial mode at a rate of approximately 1.25 Megabytes per second. When the entire packet has been transferred, the BSR is again updated (LSB cleared), per Figure 5-33, sheet 3.

Hence, the Output Packet Búffer performs two functions: (1) Receives data from the other Loop's GIB, and (2) transfers that data to the Gateway CIE's Output Queue in the B7*'s Data Memory. The first function is under control of the remote GIB and is initiated in response to an "Input Buffer Full" condition at that GIB together with the execution of the DEV 2=1 instruction, as executed by that GIB's CIE. The second function is under control of the local GIB's CIE and is initiated in response to an "Output Buffer Full" condition. This condition is signalled to the CIE when it reads the Buffer Status Register. Refer to Figure 5-33, sheet 3. The Status Register is read via the BEX 0 instruction, as executed by the CIE. The transfer to the Output Queue employs the DEV 1=2 instruction.

5.2.11.1.1 Receiving Data from the Remote GIB

The serial binary data from the remote GIB enters the Buffer Input Register (BIR) via terminal 2R on Figure 5-33, sheet 1. The BIR provides serial-to-parallel conversion of each 8-bit byte. The parallel outputs are applied to the Buffer Memory (BM 1 and BM 2) via the Buffer Input Switches (BIS-1 and BIS-2). These switches provide a direct path for the data during input to the Buffer Memory, but effectively open this input path (via the high impedance of tri-state logic) during the time that output is transferred from the Buffer Memory to the CIE Data Memory (Output Queue). The switches are controlled by the DEV 1=2 command and the resulting DEV 1=2 signal of the CIE.

Data from the remote GIB is strobed into the BIR via a 560 KHz clock, which is also received from the remote GIB. This same clock serves as the input to the Bit Counter (BC). When the BC reaches a count of eight (eight bits in the BIR), it triggers the second one shot of D3 which, in turn, generates a write pulse to the Buffer Memory (BM 1 and BM 2). This write pulse strobes the data bits from the BIR into the Buffer Memory. The output of the one shot also clears the BC so that it may begin counting the next eight bits. In addition, the one shot output increments the Buffer Address Register (BAR-1 and BAR-2) so that the next byte will be stored in the next Buffer Memory location.

The Buffer Memory consists of two memory chips (B5 and A7) each consisting of 256 locations with four bits per location, or address. Thus, BM 2 stores the four most significant bits, and BM 1 the four least significant bits, of each byte. Together, they store a complete packet, or 256 bytes. The memory chips are always in the read mode except during the pulse time (approximately 400 nsecs) of the one shot. The

one shot, as indicated above, is controlled by the BC. The write pulse (one shot output) can be applied to BM 1 and BM 2 only while DEV 1=2 is low. In effect, data may be received from the remote GIB only while the DEV 1=2 condition is not active.

When a full packet (256 bytes) has been received, the BAR's will have reached a combined count of 255, and the carry outs (CO's) will both be high. The CO's are NANDed and used for three purposes: (1) To inhibit further incrementing of the BAR's, (2) to trigger the one shot (shown on Figure 5-33, sheet 3), which in turn sets the LSB of the Status Register, and (3) to enable clearing the BAR's when the next BEX 2', A2=A2 signal is received.

With the LSB of Status Register (SR) set, the packet is ready to be transferred from the Output Packet Buffer to the CIE Output Queue. To determine that the LSB is set, the contents of the SR are periodically read into the CIE via the BEX 0 instruction and tested by the IF LST instruction.

5.2.11.1.2 Transferring Data to the CIE Output Queue

Transfer of data from the Output Buffer to the Gateway CIE Output Queue is initiated when the CIE executes the DEV 1=2 instruction. This results in the DEV 1=2 signal going high. Refer to Figure 5-33, sheet 1. DEV 1=2 going high causes the Buffer Input Switches to assume the high impedance (effectively open) state. As a result, the outputs of the Buffer Memory (BM 1 and BM 2) are applied to the inputs of the CIE Data Memory via the CIE Ancillary Board. This is accomplished via Cable Socket A3 and the cable interconnecting the GIB to the CIE Ancillary Board.

The DEV 1=2 signal is inverted and applied to the NAND gate (C1) as a low, holding the Read/Write (R/W) input of the Buffer Memory in the read state (high). The inverted DEV 1=2 signal is also applied to a NOR gate (C3) to enable the Incrementing signal to the clock input of the BAR's. Finally, the rising edge of the DEV 1=2 signal triggers a one shot (D3, pin 2) which, in turn, clears the BAR's to zero. It should be noted that the DEV 1=2 signal remains high during the transfer of the packet to the CIE Output Queue, and goes low only when the next DEV 1 instruction is executed.

With the BAR's cleared to zero, a zero address is applied to the BM. As a result the data at location zero appears on the BM data output lines. These lines are connected to the CIE Output Queue data input lines via the CIE Ancillary Board. Appropriate Memory Address Register and write pulse operation on the CIE Ancillary Board causes this data to be written into the CIE Output Queue.

While DEV 1=2 is high, an increment pulse will be generated on the CIE Ancillary Board for each CIE instruction cycle. This increment pulse will increment the Memory Address Register on the CIE Ancillary Board and will also be applied to the BAR's on the Host Interface Board. This signal is routed through several NOR gates to the clock input of the BAR's. The first NOR gate (C3, pin 5) will inhibit the signal when the BAR's reach a count of 255. The second NOR gate (C3, pin 8) will inhibit this input when DEV 1=2 is not active. The third NOR gate (F9, pin 8) permits an alternate clock (from D3, pin 5) input to the BAR's when DEV 1=2 is not active, i.e., when data is being fed into the buffer from the remote GIB.

The BARs are incremented by one count for each increment pulse applied. These incremented addresses are, in turn, applied to the BM. Hence, the data at each word location of the BM is read out in sequence to the CIE Output Queue. When the count reaches 255, the entire packet has been transferred, and the increment pulses are terminated via the CIE Ancillary Board. Also, a count of 255 in the BAR's provides an output in the form of the Combined Carry Out to the one shot (F7, pin 10) shown on Figure 5-33, sheet 3. The one shot pulses the clear input of the SR LSB. This action clears the LSB and indicates that the Output Buffer is empty. This condition will be determined by the CIE upon the next execution of a BEX 0 Instruction.

5.2.11.2 Input Packet Buffer

The Input Packet Buffer shown in Figure 5-33, sheet 2, accepts parallel binary data (eight-bit bytes) in byte-serial form from the CIE Input Queue at a rate of approximately 1.25 Megabytes per second. These eight-bit bytes are stored in the buffer until a full packet of 256 bytes have been received. When the full packet is in the buffer, the BSR (Figure 5-33, sheet 3) is updated, i.e., the Most Significant Bit (MSB) is cleared. This status, together with the execution of the DEV 2=1 instruction by the CIE, will initiate transfer (or input) of the packet to the remote GIB. When the last character of the packet is transmitted, the BSR is again updated, i.e., the MSB is set signifying Input Buffer Empty. Therefore, the next BEX 0 instruction performed by the CIE will read the BSR resulting in a determination, via an IF MST instruction, that the Input Buffer is empty.

Thus, the Input Buffer performs two functions: (1) Receives data from the CIE's Input Queue, and (2) transfers that data to the Host Processor. The first function is under control of the local Gateway CIE and is initiated in response to an Input Buffer Empty condition. This condition is signalled to the CIE when it reads the Buffer Status Register. See Figure 5-33, sheet 3. The Status register is read via the BEX 0 instruction as executed by the Gateway CIE. The second function is also under control of the local Gateway CIE processor and is initiated as a result of an Input Buffer Full condition together with the execution of DEV 2=1 instruction by the local Gateway CIE processor.

5.2.11.2.1 Receiving Data from the CIE Input Queue

Data from the CIE Input Queue can be transferred to the Input Buffer if the Input Buffer is empty. This condition is determined by the Gateway CIE via a BEX 0 command followed by an IF MST command.

Actual data transfer is initiated by the CIE's execution of the DEV 1=4 instruction and the resulting DEV 1=4 signal going high. Refer to Figure 5-33, sheet 2. The DEV 1=4 signal is inverted and applied to the Buffer Input Switches (A9 and E7) causing them to assume the normal (effectively closed) state. As a result, the data lines (1B thru 1E and 1K thru 1N) from the CIE Data Memory (Input Queue) are applied directly to the inputs of the Buffer Memory (BM 1 and BM 2). The inverted DEV 1=4 signal is also applied to one input (G1, pin 9) of a NOR gate thereby enabling the increment signal to the clock input of the BAR's. In addition, this signal is applied to a NAND gate (C1, pin 10) on Figure 5-33, sheet 3, thus enabling a clear input to the SR MSB. The DEV 1=4, prior to inversion, is applied to a NAND gate (A1, pin 2) thus enabling a write pulse input to the R/W (Read/Write) control of the Buffer Memory. Finally, the rising edge of the DEV 1=4 signal triggers a one shot (G3, pin 10) which, in turn, clears the BAR's to zero. It

should be noted that the DEV 1=4 signal remains high during the entire time that the packet is being transferred to the buffer from the CIE Input Queue. The signal goes low again when the next DEV 1 instruction is executed.

With the BAR's cleared to zero, a zero address is applied to the BM and the data on the lines from the CIE Input Queue (via the CIE Ancillary Board) are applied to location zero of the BM. Appropriate Memory Address Register operation on the CIE Ancillary Board causes data to be read out of the CIE Input Queue.

While DEV 1=4 is high, a write pulse followed by an increment pulse will be generated on the CIE ancillary board for each CIE processor instruction cycle. This write pulse is applied to the Gateway Interface Board and will strobe the data into the Buffer Memory. The increment pulse increments the Memory Address Register on the CIE Ancillary Board and the BAR's on the Gateway Interface Board. These incremented addresses are, in turn, applied to the BM. Hence, data is written into each location of the BM as it is read out of the CIE Input Queue. When the count reaches 255, the entire packet has been transferred, and the CIE Ancillary Board inhibits further counting. A count of 255 in the BAR's provides an output in the form of the Combined Carry Out to the one shot (F7, pin 2) on Figure 5-33, sheet 3. The one shot, in turn, clears the SR MSB, indicating that the Input Buffer is full. This condition will be determined by the CIE upon the next execution of a BEX 0 instruction. Also, the packet will be transferred to the remote GIB upon the next execution of a DEV 2=1 Instruction.

5.2.11.2.2 Transferring Data to the Remote GIB

Transfer of the 256-byte packet of data from the Input Buffer to the Remote GIB can be accomplished only when the DEV 1=4 signal is low. Refer to Figure 5-33, sheet 2. In this condition, the R/W input of the BM is held high (read state for BM), the increment input to the BAR's is inhibited, a BAR's clock input from the Bit Counter (BC) is enabled, the Buffer Input Switches (BIS's) are effectively opened, and a NAND gate (E1, pin 11), shown on Figure 5-33, sheet 3, is enabled to permit setting the MSB of the SR.

Transfer of data from the Input Buffer to the remote GIB is actually initiated via execution of the DEV 2=1 instruction by the local Gateway CIE. The DEV 2'=1 signal (Figure 5-33, sheet 2) goes low for one instruction time, and if the Combined Carry Out (CCO) signal is also low (BAR's set at 255) then the DEV 2'=1 signal clears the BAR's to zero. As the DEV 2'=1 signal returns to the high level, it triggers the BOR One Shot which, in turn, provides a load pulse to the BOR. (Note that the load pulse to the BOR must be greater than 900 nsecs but less than 1200 nsecs.) Hence, the contents (eight bits) of location zero of the Buffer Memory are loaded into the BOR and are ready for transmission in serial form to the remote GIB.

In addition to zeroing the BAR's and loading the first word into the BOR, the DEV 2'=1 signal and the IB full' signal are applied to the NOR gate F9 on Figure 5-33, sheet 3. The output from this gate presets flip-flop E5, Figure 5-33, sheet 2. The output of this flip-flop, applied to pin 2 of flip-flop E7, results in a high applied to pin 4 of NAND gate D1. Therefore, clock (CKO) is enabled to pin 2 of BOR and data is clocked out of BOR to the remote GIB. Clock is also applied to BC, and when BC reaches a count of eight, a falling edge is applied to pin 3 of F9 and pin 1 of G3. This results in the BAR's being incremented and a load pulse being

applied to pin 1 of BOR. The load pulse must be sufficiently long to increment the address to BM 1 and BM 2, the output data from BM 1 and BM 2 to become valid and loading of BOR to be completed. This total time must be between 900 and 1200 nanoseconds. An output from pin 13 of G3 clears G7 and allows G7 to reinitiate counting. The next eight clocks output the next data word from BOR and the cycle repeats. After the output of 256 characters in this manner, the BAR's carry outs are active. They are gated and applied to pin 2 of F7 on Figure 5-33, sheet 3. The output of F7 presets the MSB of E9 thereby indicating Input Buffer empty. The signal from E9, pin 5, is applied to pin 13 of NAND gate D1 on Figure 5-33, sheet 3. When the next high is output from pin 11 of the BC (G7), the input to the one shot (F3) goes low. The output from the one shot clears flip-flop E5 causing its output to E7 to go low. The output of E7 goes low on the next clock and thereby clock CKO is inhibited to BOR and to the BC. Hence, output from the BOR to the remote GIB is completed.

5.2.11.3 Buffers Status Register

The Buffers Status Register (BSR) is a two-bit register consisting of two flip-flops. (Refer to Figure 5-33, sheet 3.) The LSB stores the status of the Output Buffer and the MSB stores the status of the Input Buffer. The LSB is either cleared or set by the appropriate combination of DEV 1=2 and COOB or DEV 1=2' and COOB, respectively. The MSB is either cleared by the combination of DEV 1=4 and COIB or set by the combination of DEV 1=4' and COIB. Note that both COIB and COOB must always be greater than 1 microsecond; ideally 1.5 μsec.

Setting both LSB and MSB is inhibited while the BEX 0' signal is low, the low occurring during the time that the contents of the BSR is being read (via terminal 1Q) by the Host CIE via the BEX 0 command. When the BSR is read into the CIE's B register, via the BEX 0 command, the content of LSB appears in the Least Significant Bit as well as all odd numbered bits of the B register. The content of MSB appears in the most significant bit as well as all even numbered bits of the B register. During the BEX 0 instruction, which involves eight clock pulses, the contents of the BSR are shifted circularly so that they end up in their original locations.

When LSB is cleared or MSB is cleared, a low level is applied to C3, pin 2, or F9, pin 12, respectively. These cleared conditions represent Output Buffer empty and Input Buffer full, respectively. The first of these is gated with BEX 2', A2=A2 and used to clear the BC on Figure 5-33, sheet 1. The second is gated with DEV 2'=1 and used to preset the flip-flop E5 on Figure 5-33, sheet 2. The results of these actions were discussed earlier in paragraphs 5.2.11.1 and 5.2.11.2.

5.2.12 CRT INTERFACE BOARD

The CRT Interface Board permits an ESM CIE to interface with a 9600 Baud CRT terminal (e.g., Burroughs TD 802) or a 300 Baud data terminal, and to send or receive ASCII characters (start bit, seven data bits, a parity bit, and a stop bit) in an asynchronous mode (see Figure 5-35) at 9600 bits per second or 300 bits per second.

The CRT Interface Board consists of: (1) An output (with respect to the CRT) Character Buffer, (2) an input (with respect to the CRT) Character Buffer, and (3) a Buffer Status Register.

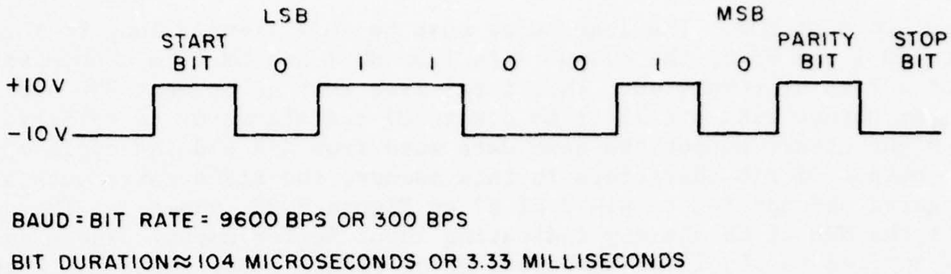


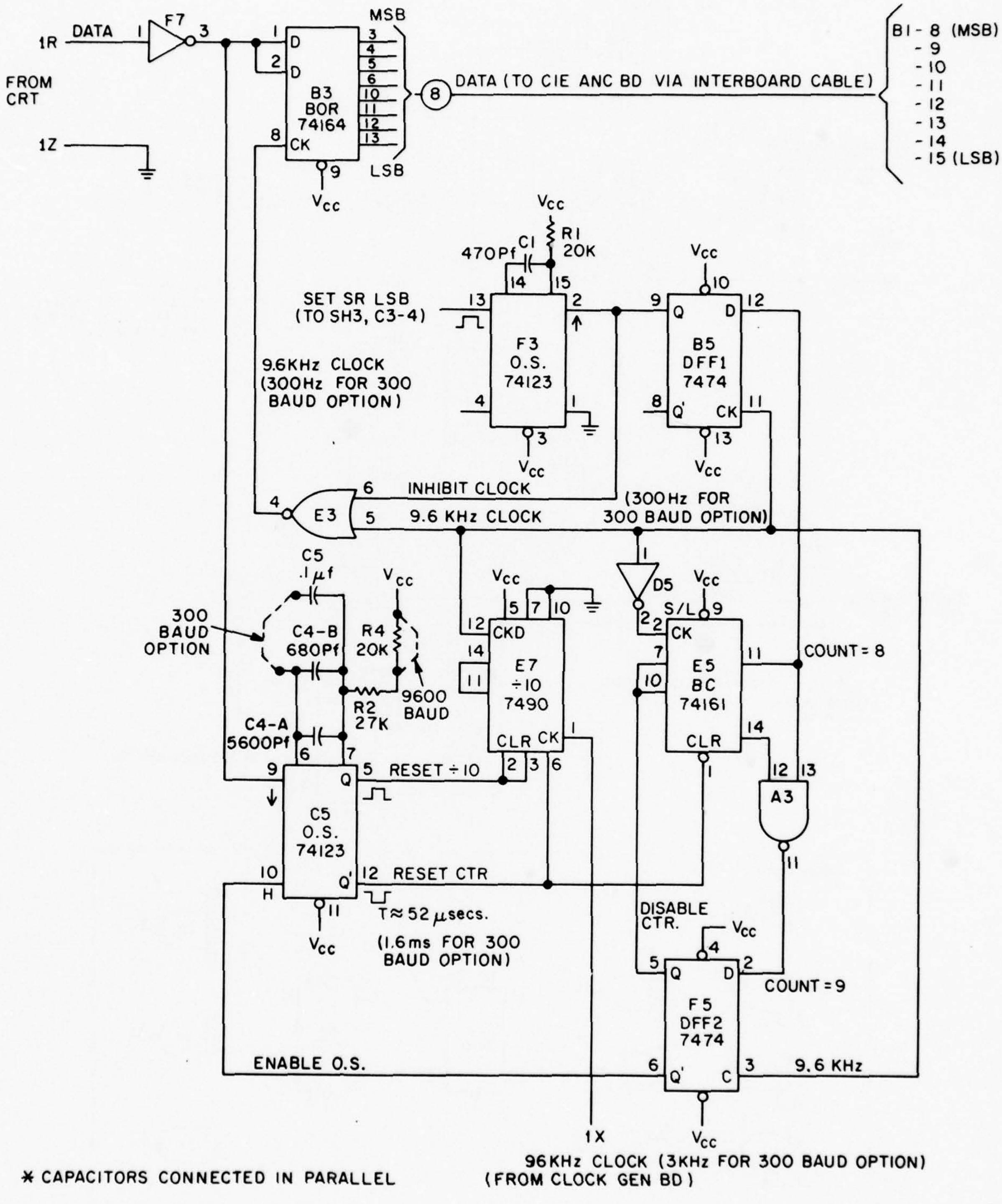
Figure 5-35. Asynchronous Data Signal

The following description deals specifically with the 9600 Baud configuration. For the 300 Baud configuration, or option, the referenced clock rates and pulse durations are altered by a factor of 32. Option configuration details are provided on Figure 5-36 and 5-37, and are summarized on Figure 5-37, sheet 2.

5.2.12.1 Output Character Buffer

Refer to Figure 5-36, sheet 1, for the following circuit descriptions. A 96 KHz clock (3 KHz for 300 Baud option) is continually present at 1X, supplied from the Clock Generator Board. Therefore, a 9.6 KHz output (300 Hz for the 300 Baud option) is always being fed from the ÷ 10 counter (E7) to the Binary Counter (E5) and to the Delay Flip-Flops (B5 and F5). The Binary Counter upon reaching a count of eight inhibits clock to the Buffer Output Register (B3). When reaching a count of nine the Binary Counter enables the one shot (C5). The Delay Flip-Flops provide a delay equal to one-half the period of the 9.6 KHz (or 300 Hz) signal.

With the clock to the Buffer Output Register inhibited and the one-shot (C5) enabled, an asynchronous data signal, having the form indicated on Figure 5-35, can be received at 1R and can be stored in the Buffer Output Register. That is, the first transition of the received signal will start the clock to B3. The asynchronous signal consists of a start bit (always positive), eight data bits (least significant bit through most significant bit, plus parity bit) and a stop bit (always negative). Note that the signals received from the CRT alternate between +10V and -10V, per EIA RS-232-C. The Line Receiver (F7) converts the levels to standard TTL levels (i.e., the +10V becomes 0V and the -10V becomes +5V). The positive-going leading edge of the start bit, present at 1R, triggers the one shot (C5), assuming that the one shot is enabled. The outputs from the one shot (C5) clear the Counters (E5 and E7) and hold them at zero for the duration of the outputs. The one shot must provide outputs with a duration of approximately 52 microseconds (1.6 milliseconds for 300 Baud option). With the counters zeroed, the Clock Inhibit and the One-Shot Enable signals are both negated. Hence, clock is applied to the Buffer Output Register, and the one shot ignores any inputs from the Line Receiver. Note that the first clock to the Buffer Output Register occurs approximately 156 microseconds (one and one-half bit times) after the rising edge of the start pulse. As a result, the first clock strobes the LSB of the received data signal. Eight clocks later the eight data bits are contained in the Buffer Output Register, and the Inhibit Clock signal interrupts clock to the Buffer Output Register and triggers



* CAPACITORS CONNECTED IN PARALLEL

Figure 5-36. CRT Interface Board Buffer Logic (Sheet 1 of 3)

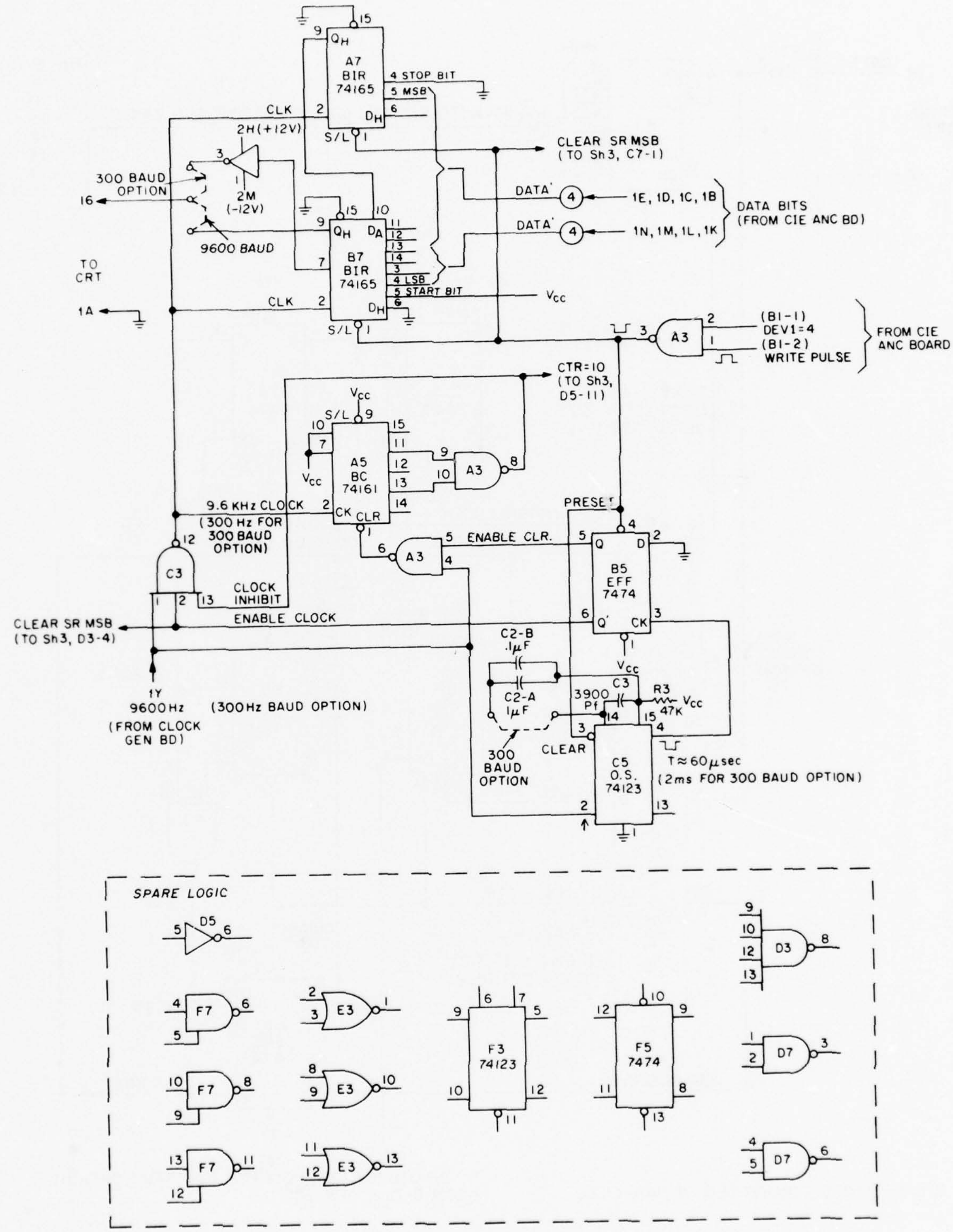
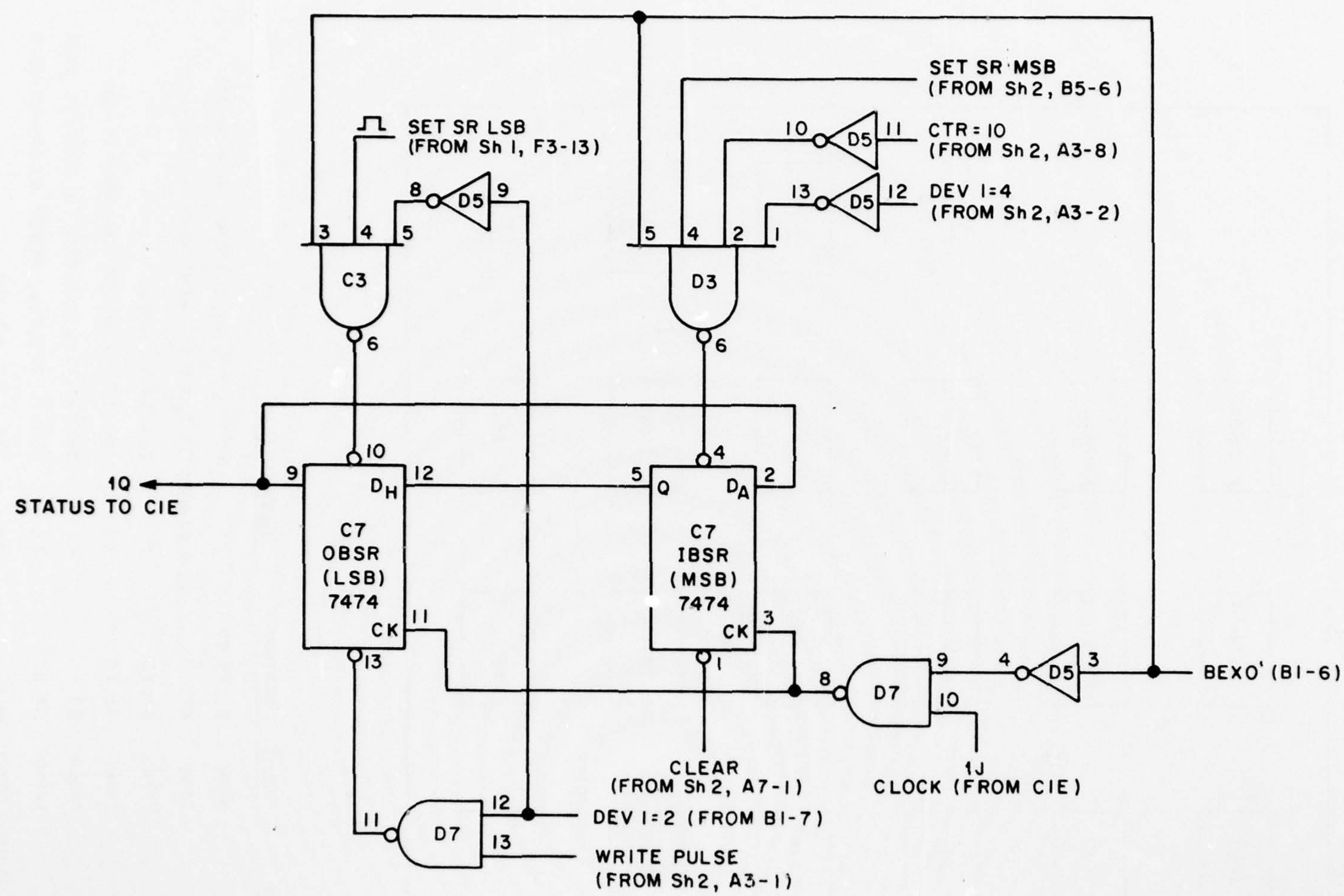


Figure 5-36. CRT Interface Board Buffer Logic (Sheet 2 of 3)

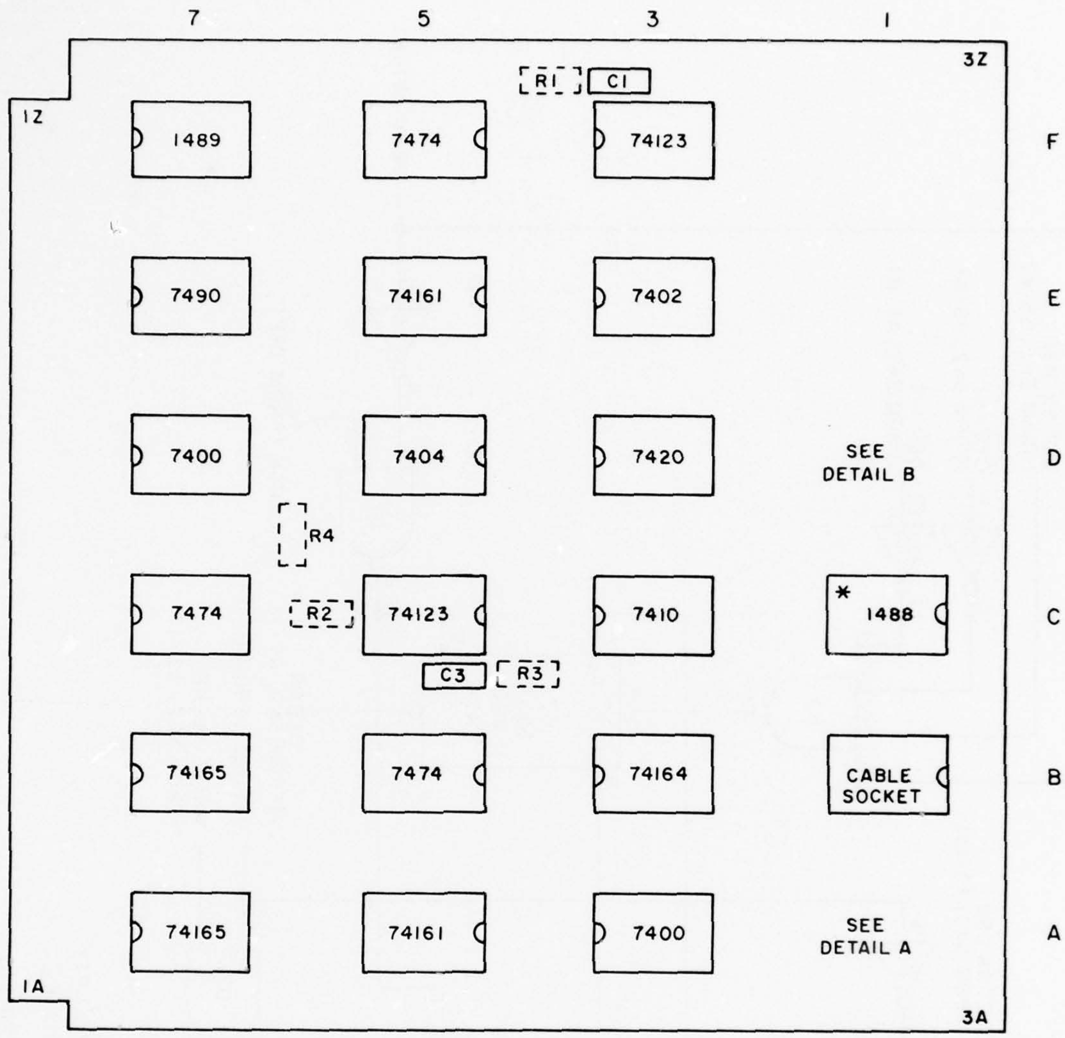


NOTE:

MSBT ≡ SET D_A ≡ INPUT BUFFER REGISTER EMPTY
CLR D_A ≡ INPUT BUFFER REGISTER FULL

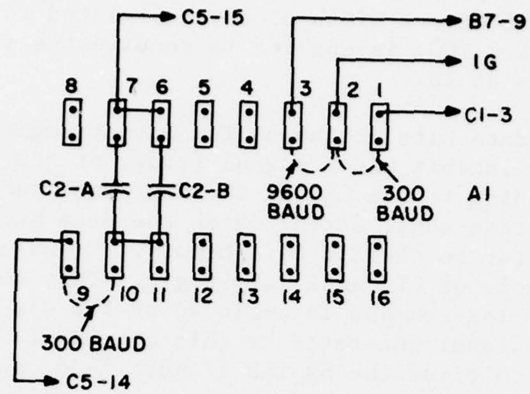
LSBT ≡ SET D_H ≡ OUTPUT BUFFER REGISTER FULL
CLR D_H ≡ OUTPUT BUFFER REGISTER EMPTY

Figure 5-36. CRT Interface Board Buffer Logic (Sheet 3 of 3)

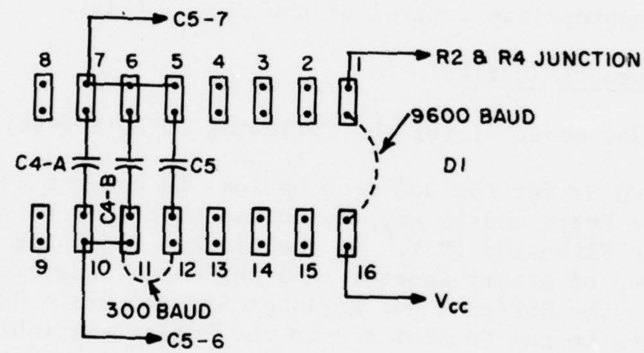


IDENT	LOCATION	IDENT	LOCATION	IDENT	VALUE
1489	F7	7474	B5, F5, C7	C1	470 Pf, 10% TOL., CENTRALAB # DD-471
7400	A3, D7	7490	E7	C2-A, C2-B, C5	0.1μF, 10% TOL. KEMET# CK05-BX-104K
7402	E3	74123	C5, F3	R1	20K, 1/8 W, 5% TOL.
7404	D5	74161	A5, E5	C4-B	680 Pf, 10% TOL., CENTRALAB # DD-681
7410	C3	74164	B3	C4-A	5600 Pf, 10% TOL., KEMET # CK05-BX-562K
7420	D3	74165	A7, B7	C3	3900 Pf, 10% TOL., KEMET # CK05-BX-392K
*1488	C1 (FOR 300 BAUD OPTION ONLY)			R2	27K, 1/8W, 5% TOL.
				R3	47K, 1/8W, 5% TOL.

Figure 5-37. CRT Interface Board, Parts Layout Diagram and Parts List (Sheet 1 of 2)



DETAIL "A"



DETAIL "B"

CONFIGURATION FOR 300 BAUD OPERATION

1) REMOVE 9600 BAUD JUMPERS
2) ADD A1-9 TO A1-10 JUMPER
3) ADD A1-1 TO A1-2 JUMPER
4) ADD D1-11 TO D1-12 JUMPER
5) ADD C1 CHIP, 1488

CONFIGURATION FOR 9600 BAUD OPERATION

1) REMOVE 300 BAUD JUMPERS
2) ADD A1-2 TO A1-3 JUMPER
3) ADD D1-1 TO D1-16 JUMPER
4) REMOVE C1 CHIP, 1488

Figure 5-37. CRT Interface Board, Parts Layout Diagram and Parts List (Sheet 2 of 2)

the Status Register One Shot (F3). This, in turn, sets the LSB (least significant bit) of the Status Register (C7), shown on Figure 5-36, sheet 3, indicating that the Buffer Output is full. After the ninth clock, as related to the stop bit of the data signal, the first one shot (C5) is enabled to receive the rising edge of the next start bit, as it appears at 1R.

It should be noted that the data bits in the Buffer Output Register remain stable only between the time of the Inhibit Clock signal (i.e., at the end of the parity bit) and the clock corresponding to the LSB of the next received character. This is a period of about 260 microseconds, during which the data must be transferred from the Output Buffer Register to the CIE Data Memory. Transfer is accomplished via the CIE B7* and its associated CIE Ancillary Logic. This Logic is described in paragraph 5.2.7. The DEV 1=2 command is employed by the CIE B7* as the means of this transfer. The DEV 1=2 signal generated by this command is also gated, via D7, with the write pulse signal to clear the SR LSB (Figure 5-36, sheet 3), thereby indicating that the Buffer Output Register is empty. The write pulse signal is also used by the CIE Data Memory.

It should be noted that the start bit and stop bit are stripped from each received data character by appropriate control of the clock signal.

5.2.12.2 Input Character Buffer

Refer to Figure 5-36, sheet 2, for the following circuit descriptions.

A 9.6 KHz clock (300 Hz for the 300 Baud option) is continually present, at 1Y, from the Clock Generator Board and is applied to one shot (C5) which, in turn, provides clock to the Enable Flip-Flop (B5). In the clocked mode, the flip-flop's outputs inhibit the clearing of Binary Counter (A5) while enabling clock input to the Counter (A5) and to the Buffer Input Register (A7 and B7). When the counter reaches 10, the clock inputs to the Counter and to the Buffer are inhibited. The Counter stops, and the MSB (most significant bit) of the SR (C7 on Figure 5-36, sheet 3) is set indicating that the Buffer Input Register is empty. The Buffer is now ready to be loaded from the CIE Data Memory via the CIE B7* and its associated Ancillary Logic. This Logic is described in paragraph 5.2.7.

Data from the CIE Data Memory is transferred to the input buffer via the DEV 1=4 instruction. This instruction generates both the DEV 1=4 signal and the Write Pulse signal shown on Figure 5-36, sheet 2. These signals are gated (via A3) to generate the Load Pulse for the Buffer Input Register, thereby strobing the data bits (in parallel) and the start and stop bits into the buffer. This pulse also clears the MSB of the Status Register (Figure 5-36, sheet 3), indicating that the Buffer Input Register is full. This same pulse presets the Enable Flip-Flop (B5). One flip-flop output enables the next positive clock to clear the counter and the other output inhibits the clock input to the counter. Clearing the counter causes the other clock inhibit, previously generated by Count = 10, to be removed.

The same pulse that presets the flip-flop also clears (output held high) the one shot (C5) preventing possible undesired clocking of the flip-flop before Buffer loading is completed. After this Load/Preset/Clear pulse decays, the next rising edge of the 9600 Hz clock (300 Hz for the 300 Baud option) triggers the one shot which, in turn, clocks the flip-flop after approximately 60 microseconds (2 milliseconds for the 300 Baud option). The resulting flip-flop outputs inhibit further clearing of the flip-flop and enable clock to the counter as well as to the Buffer Register. As

a result, ten consecutive clock pulses are applied to the Buffer (A7 and B7) which shifts out ten bits (start bit, LSB through MSB, parity bit and stop bit) at pin B7-7 and 9. This signal has the format and polarity shown on Figure 35 and varies between 0V and 5V. When ten clocks are counted by the counter, additional clock inputs are inhibited and the MSB of the Status Register (Figure 5-36, sheet 3) is set. Hence, the Input Buffer is ready to receive another 8-bit word from the CIE.

5.2.12.3 Buffers Status Register

Refer to Figure 5-36, sheet 3, for the following circuit descriptions.

The Buffers Status Register (C7) is a two-bit circulating register with associated logic for setting and clearing the bits according to the rules listed on Figure 5-36, sheet 3. The two-bit contents of this register are clocked out at 1Q and into the "B" register of the CIE B7* via the BEX 0 command. Clock pulses, apparent at 1J, are supplied from the CIE B7* and are gated to the register by the BEX 0 signal, a product of the BEX 0 command. Eight clock pulses are provided, thus transferring the LSB to all odd-bit locations of the CIE "B" register, and the MSB to all even-bit locations of the CIE "B" register. The CIE B7* then tests the contents of the "B" register using the LST and MST Condition Test Instructions to determine the actual status of the Buffer Input and Buffer Output Registers. The BEX 0 signal also inhibits setting of the flip-flops (C7) while the BEX 0 command is active, prohibiting change of status during output.

5.2.13 LOADER BOARD AND LOADER ANCILLARY BOARD

The Loader Board (LB) (Figures 5-38 and 5-39) and Loader Ancillary Board (LAB) (Figures 5-40 and 5-41) function together to facilitate loading CIE Control memories directly from the Host Processor PDP-11/40. The LAB accepts serial data and clock at 2G and 2H (Figure 5-40, sheet 1) from the PDP-11/40 and gates them to the LB. The LB, upon receiving 16 data bits (one PDP-11/40 word), applies twelve of these bits in parallel to the data inputs of one of up to four CIE control memories, as selected by the cabinet Panel-Mounted Switches. The LAB interfaces with these switches, and as a result of their settings: (1) Enables the loading process, (2) selects the CIE Data Memory to be loaded, (3) selects the initial memory address by clearing the B7*'s Memory Address Register to zero, (4) increments the memory address for each 12-bit instruction word to be loaded, (5) strobes the instruction word into the selected memory location, and (6) prohibits the execution of instructions while loading.

In addition, the LAB interfaces the cabinet Panel-Mounted Maintenance Switches (lower two rows) to the appropriate CIE and NCU B7*'s.

5.2.13.1 Loading CIE Memories

Data and clock, at 560 Kbps and 560 KHz, respectively, are routed from the PDP-11/40, via its M1710 interface and interconnecting cable, to the Host Interface Board (described in paragraph 5.2.9) of ESM Cabinet Number 2. The Host Interface Board in that cabinet provides isolation and buffering (per paragraph 5.2.9.4) for the data and clock which is then routed to the Loader Ancillary Board in ESM Cabinets Numbers 1, 2 and 3. This data and clock are received on terminals 2G and 2H, respectively, of the LAB (Figure 5-40, sheet 1). When the panel-mounted LOAD

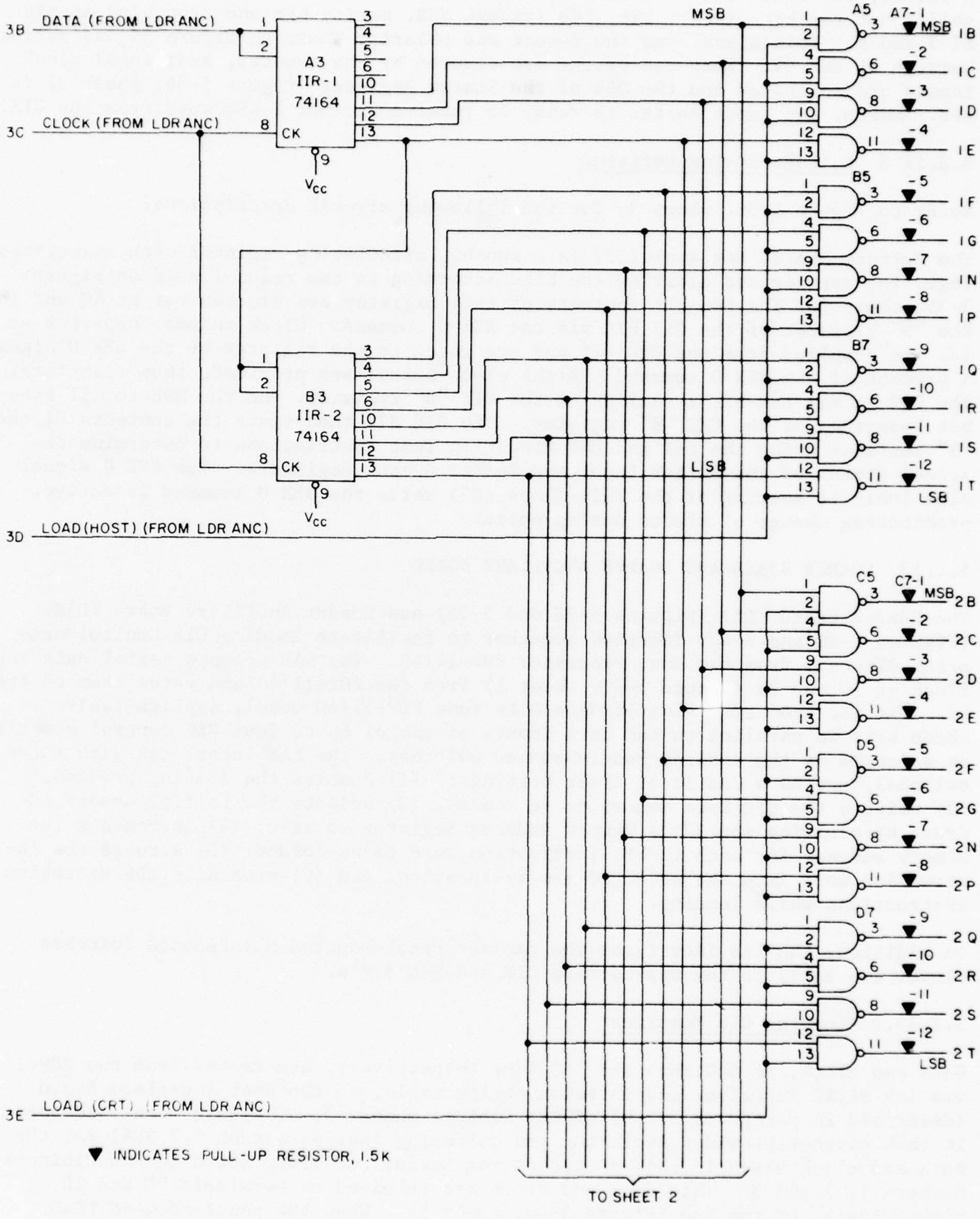


Figure 5-38. Loader Board, Logic Diagram (Sheet 1 of 2)

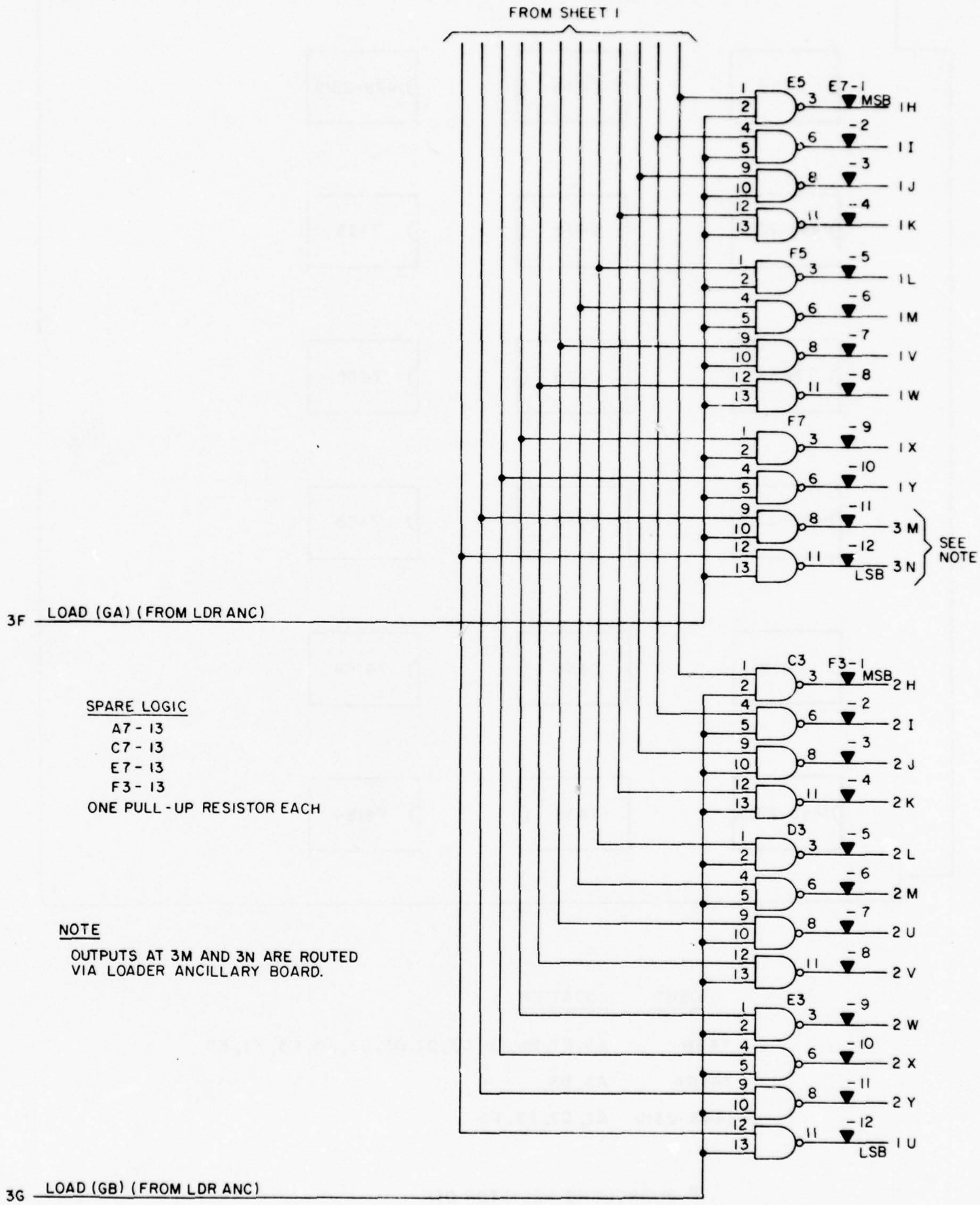
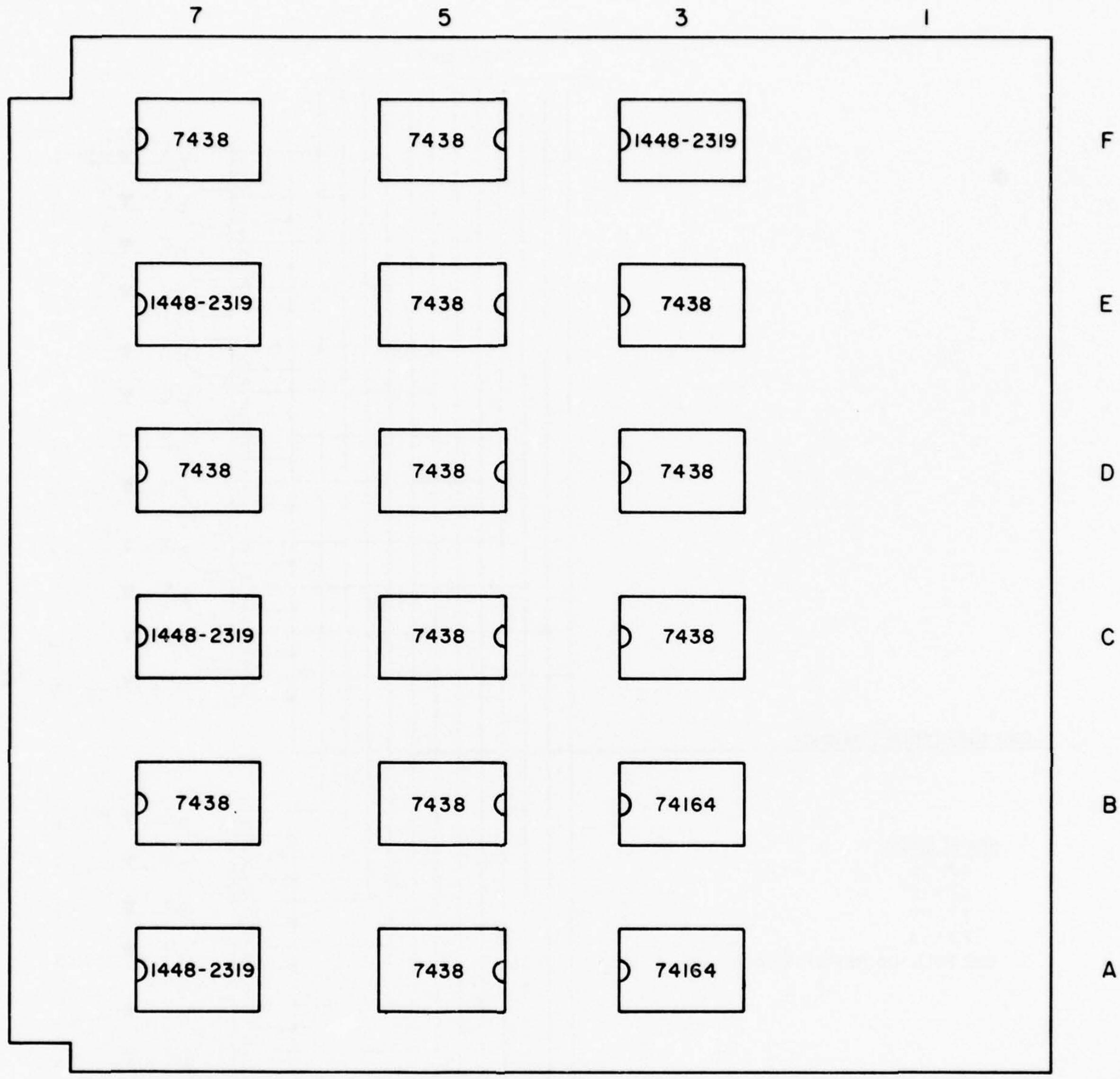


Figure 5-38. Loader Board, Logic Diagram (Sheet 2 of 2)



IDENT	LOCATION
7438	A5, B7, B5, C5, C3, D7, D5, D3, E5, E3, F7, F5
74164	A3, B3
* 1448-2319	A7, C7, E7, F3

* BURROUGHS RESISTOR DIP

Figure 5-39. Loader Board, Parts Layout Diagram and Parts List

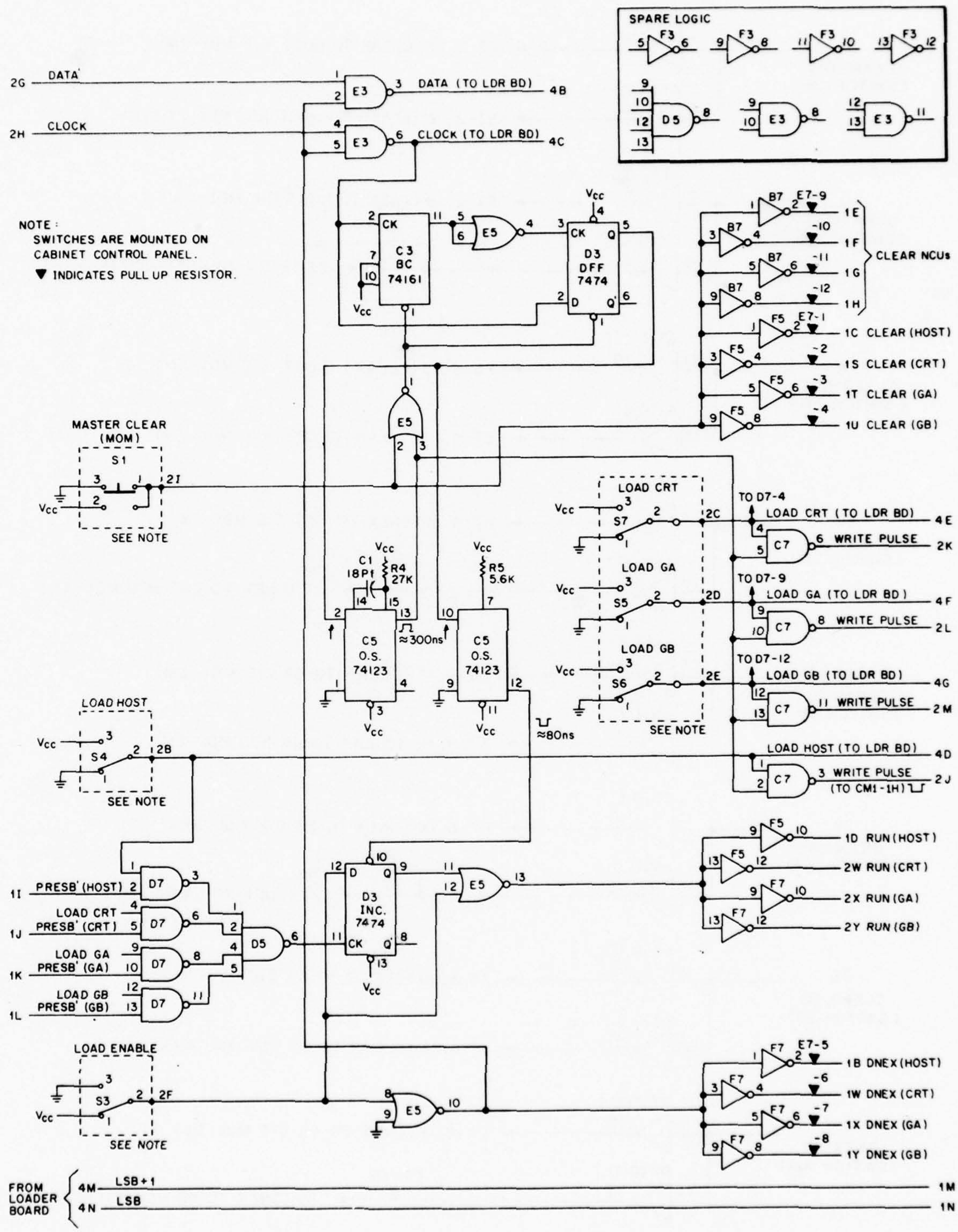


Figure 5-40. Loader Ancillary Board, Logic Diagram (Sheet 1 of 2)

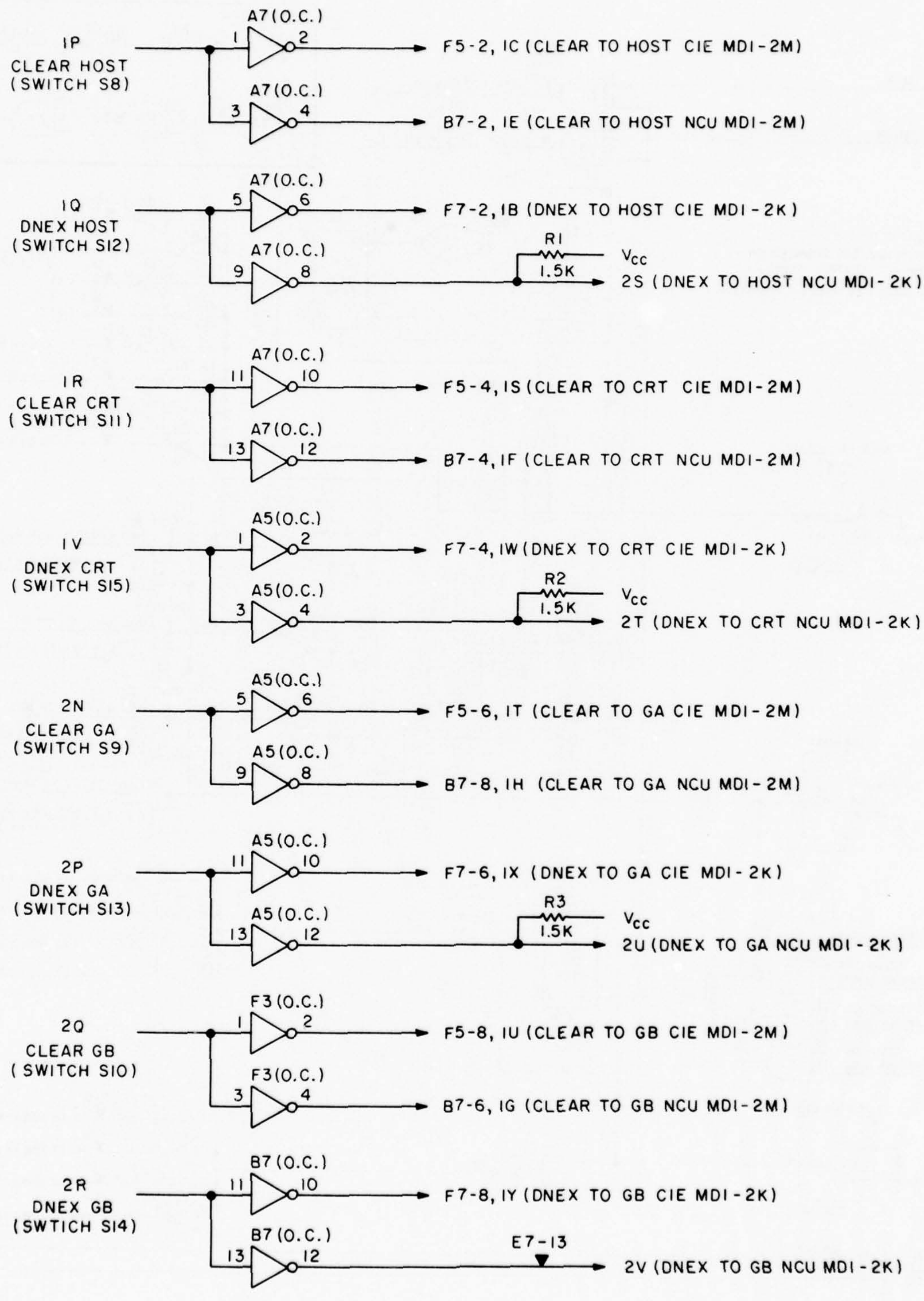
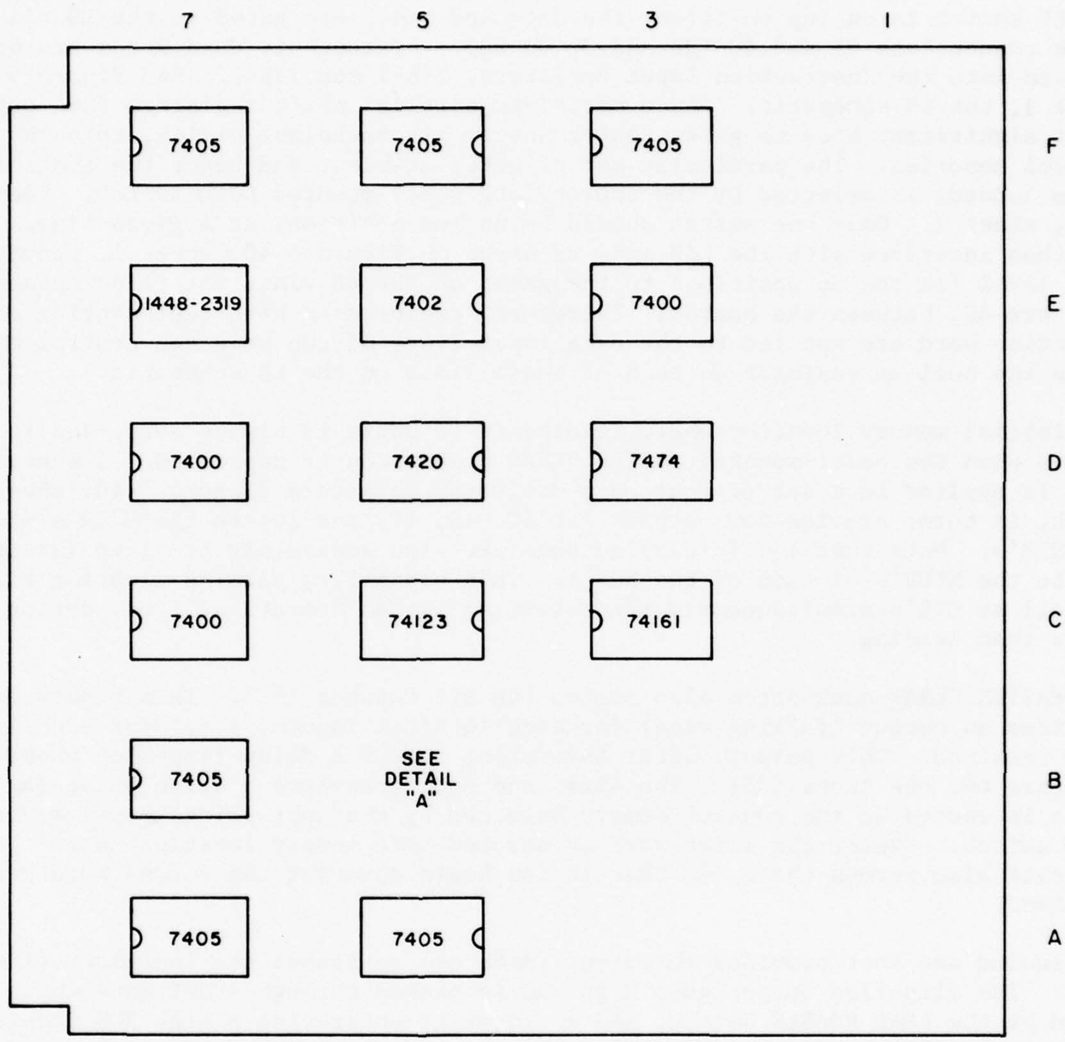


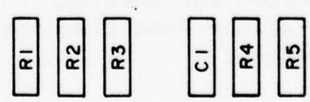
Figure 5-40. Loader Ancillary Board, Logic Diagram (Sheet 2 of 2)



IDENT	LOCATION
7400	C7, D7, E3
7402	E5
7405	A5, A7, B7, F3, F5, F7
7420	D5
7474	D3
74123	C5
74161	C3
* 1448-2319	E7

* BURROUGHS RESISTOR DIP

DETAIL "A"



R1, R2, R3	1.5K, 1/8W, 10% TOL.
R4	27K, 1/8W, 5% TOL.
R5	5.6K, 1/8W, 5% TOL.
C1	18 PF, 10% TOL., CENTRALAB # DD-180

Figure 5-41. Loader Ancillary Board, Parts Layout Diagram and Parts List

ENABLE switch is on (up position) the data and clock are gated to the LB via Front Plane connections 4B and 4C (3B and 3C on LB). Sixteen-bit data words are now clocked into the Instruction Input Registers, IIR-1 and IIR-2. See Figure 5-38, sheet 1, the LB schematic. These serial-to-parallel shift registers feed out the 12 least significant bits to gates that connect, via backplane wiring, to each of four control memories. The particular set of gates enabled, and hence the control memory to be loaded, is selected by the appropriate panel-mounted LOAD Switch. See Figure 5-40, sheet 1. Only one switch should be on (up position) at a given time. These switches interface with the LAB and, as shown on Figure 5-40, sheet 1, provide a high level (in the up position) to the gates on the LB via Front Plane connections (4D thru 4G) between the boards. Therefore, twelve data bits representing an instruction word are applied to the data input lines of the selected control memory. (Note the pull-up resistor on each of these lines on the LB schematic.)

The initial memory location where loading is to begin is always zero, and is established when the panel-mounted MASTER CLEAR pushbutton is depressed. A momentary high is applied to a set of four open-collector inverters (Figure 5-40, sheet 1) which, in turn, provide low outputs (at 1C, 1S, 1T, and 1U) to the MPCR's of each of the CIE's. Note that low (clear) outputs are also separately provided (at 1E thru 1H) to the MPCR's of each of the NCU's. This capability permits clearing all NCU's as well as CIE's simultaneously when starting system operation, i.e., during times other than loading.

The MASTER CLEAR pushbutton also zeroes the Bit Counter (BC). This binary counter provides an output (falling edge) for each 16 clock inputs, i.e., for each 16-bit word received. This output, after inversion, clocks a delay flip-flop whose output triggers two one shots (C5). The first one shot generates a write pulse ($\approx$ 300 ns) which is routed to the control memory selected by the appropriate panel-mounted LOAD switch. Hence, the first word is strobed into memory location zero. The first one shot also zeroes the BC so that it can begin counting the second word being received.

The second one shot provides an output ($\approx$ 80 ns) to preset the Increment (INC) flip-flop. The flip-flop output goes high and is passed through a NOR gate which is enabled by the LOAD ENABLE switch, and an inverter to provide a high RUN level to each of the CIE's. Hence, all CIE's step through one instruction cycle, thereby incrementing their respective MPCR's. The RUN signal goes low at the end of each instruction cycle because the INC flip-flop is reset by the rising edge of the PRESB' signal. That is, the PRESB' signal, corresponding to the CIE control memory that is selected for loading, is gated (via D7 and D5) to the clock input of the INC flip-flop. At the same time the LOAD ENABLE switch applies a low to the data input of the flip-flop.

As a result of the above described operations, a selected control memory is loaded from the PDP-11/40. Initially, all switches must be set according to the instructions provided in paragraph 4.3 of the ESM Operators Manual prior to initiating data transfer from the PDP-11/40. Up to 4K instructions can be loaded into each CIE's control memory in this manner. MPCR incrementing stops after the last instruction is loaded, but at a multiple of 128 instructions. That is, the PDP-11 always transfers multiples of 128 instructions. Dummy words (all zeros) are placed between the last instruction and the next multiple of 128.

5.2.13.2 Maintenance Switch Interfacing

The bottom two rows of the cabinet panel-mounted switches are interfaced to appropriate logic circuits via gates located on the LAB. See Figure 40, sheet 2. Each CLEAR switch provides either a high (clear condition) or a low (normal condition) level to the inputs of two inverters. The output of one inverter is connected to the MPCR clear input of the CIE B7*; the output of the other inverter is connected to the MPCR clear input of the NCU B7*. Hence, in the up position, the MPCR's of the indicated pair of B7*'s are cleared to zero.

Each DNEX switch provides either a high (DNEX condition) level or a low (normal condition) level to the inputs of two inverters. The output of one inverter is connected to the DNEX input of the CIE B7*; the output of the other inverter is connected to the DNEX input of the NCU B7*. Note the pull-up resistor required on the output to each NCU B7*. Hence, in the up position, the indicated pair of B7*'s are prohibited from executing instructions.

This DNEX status is actually achieved by clearing the contents of B7* Instruction Register to zeros. It should be noted that all zeros in the Instruction Register represents the valid instruction: DEV 0=0. Therefore, in the DNEX mode, the DEV 0=0 instruction is actually active.

5.2.14 MONITOR

The monitor provides the capability for direct monitoring and operation of a B7* microprocessor as employed in the ESM. It can be used with any B7* (NCU or CIE) in any of the three ESM cabinets. However, it must be plugged into the appropriate CMON or NMON card slot. See Figure 2-4 and Table 2-1. Its use and operation are described in paragraph 4.1.4 of the User Manual for the ESM.

The following description of the Monitor is organized by functions as follows:

a. Control of B7*

b. Monitoring of B7*

c. Instruction loading

It should be noted that each function, as described, applies to either the CIE or the NCU B7*, depending upon which card slot (CMON or NMON) the monitor is plugged into. See Figure 2-4 and Table 2-1.

5.2.14.1 Control of B7*

The monitor provides the following control capabilities, via toggle switch or pushbutton, relative to the B7*:

a. DNEX - Don't Execute, or Execute, as selected.

b. CLEAR - Clear MPCR and AMPCR of the B7*.

c. START - Start B7* Execution when in the RUN Mode; single-step B7* when in the SNGL mode.

d. SNGL/RUN - Select single step or RUN Mode for B7*.

Refer to Figure 5-42, sheet 1, for the following discussion:

The DNEX switch is open in the down position, resulting in a high level being present at output pin 2K of the Monitor Board. This output is routed (via backplane wiring) to the clear input of either the CIE B7* or the NCU B7* Instruction Register, depending upon which slot it is plugged into. Hence, the appropriate Instruction Register is allowed to execute. However, when the DNEX switch is in the up position, a ground (low) is routed to the clear input of the Instruction Register, thereby clearing the register and prohibiting instruction execution. It should be noted that all zeros in the Instruction Register represents the instruction DEV 0=0. Therefore, in the DNEX mode, the DEV 0=0 instruction is actually active.

The output of the DNEX switch also applies either a high or low (depending on switch position) to Monitor Board output pin 1L. The actual level resulting at 1L, however, is also dependent upon the position of the SNGL/RUN switch. That is, when either the DNEX switch or the SNGL/RUN switch is in the up (closed) position, a low is present at 1L. This level (at 1L) is routed (via backplane wiring) from the NCU Monitor only to pin 1L of the LIU Board. This low level is required by the LIU Board to enable its operation when the NCU Monitor is being operated with the DNEX switch or the SNGL/RUN switch, or both, in their up position.

The output of the CLEAR momentary contact pushbutton switch, when depressed, results in a low at output pin 2M of the Monitor Board. This output is routed, via backplane wiring, to the clear input of the MPCR and AMPCR of the CIE or NCU B7*. Hence, depressing the CLEAR switch clears both the MPCR and the AMPCR to zero.

The START momentary contact pushbutton switch, when depressed, changes the input states to the first J-K master-slave flip-slop of E3. Clock from the B7* (NCU or CIE) is applied continually to the flip-flops via pin 1B of the Monitor Board. On the falling edge of the clock (with the START button depressed) the outputs of the first flip-flop change. Hence, the input to pin 2 of the NAND gate C3 changes from a low to a high. Since the other input (pin 1) to the NAND gate is already high, the gate output will go low. The next falling edge of the clock will cause the second flip-flop to change output states. The falling edge of the next clock pulse will cause the output of the third flip-flop to change state. Hence, the input at pin 1 of NAND gate C3 wili go low and its output will be high. Therefore, depressing the START switch produces a low at the output of C3 that is two clock pulses in duration. This pulse is used to set the latch formed by the gates of C3 pins 8 through 13.

With the SNGL/RUN switch in the SNGL (up) position, a high is applied to input pin 9 of latch C3 and a low is applied to input pin 13. This results in a low at pin 6 of C3. Now, when the START button is depressed, the low from pin 3 of C3 is routed, via terminals 1 and 2 of switch S16, to pin 4 of C3. Hence, the output of C3 at pin 6 goes high for two clock periods. This pulse is routed from pin 1Y of the Monitor Board to the RUN input of the B7*. Hence, the B7* operates for one instruction cycle as a result of each depression of the START pushbutton. Also, the MPCR of the B7* increments as a result of each depression of the START pushbutton.

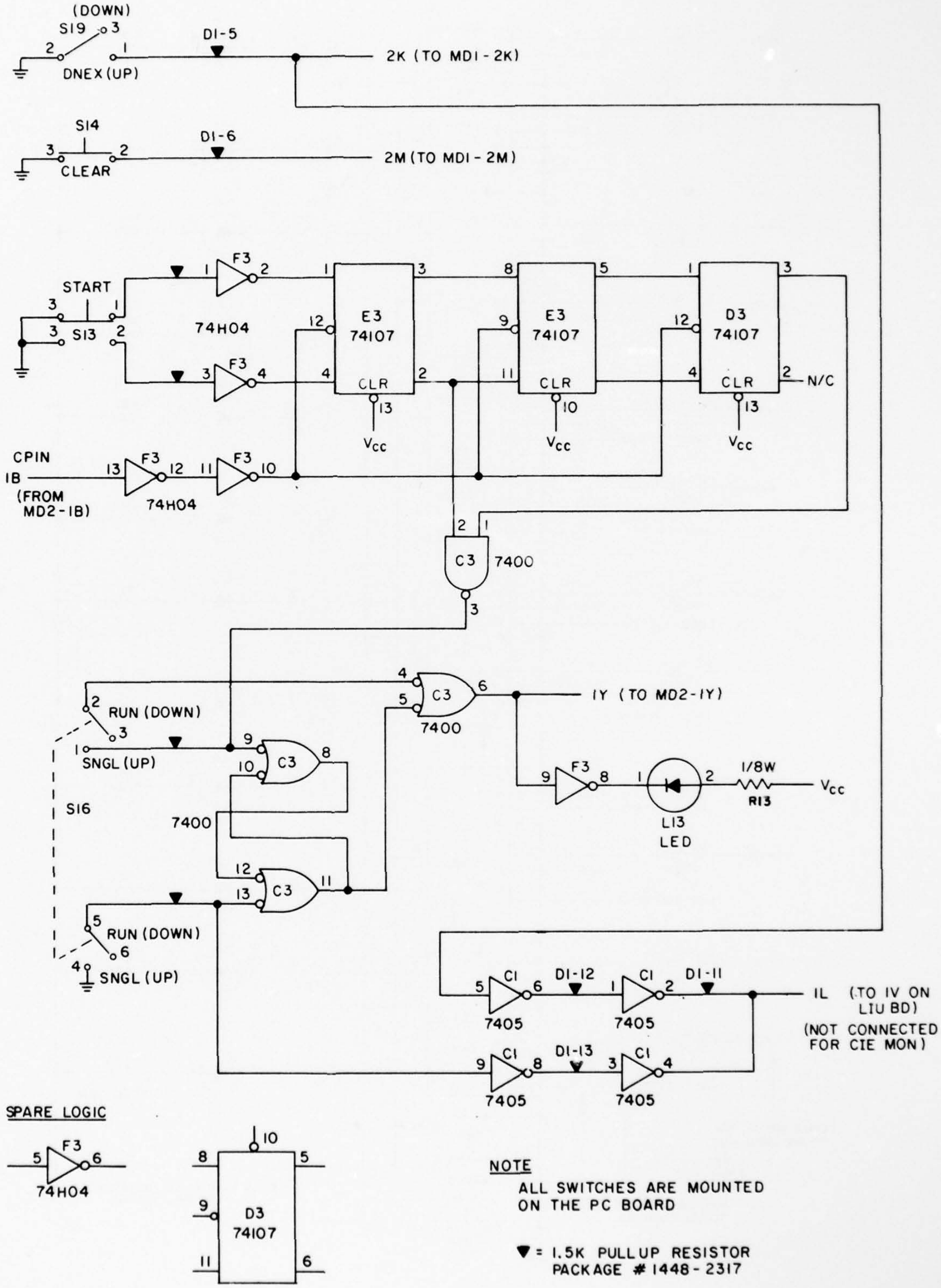


Figure 5-42. Monitor Board, Logic Diagram (Sheet 1 of 3)

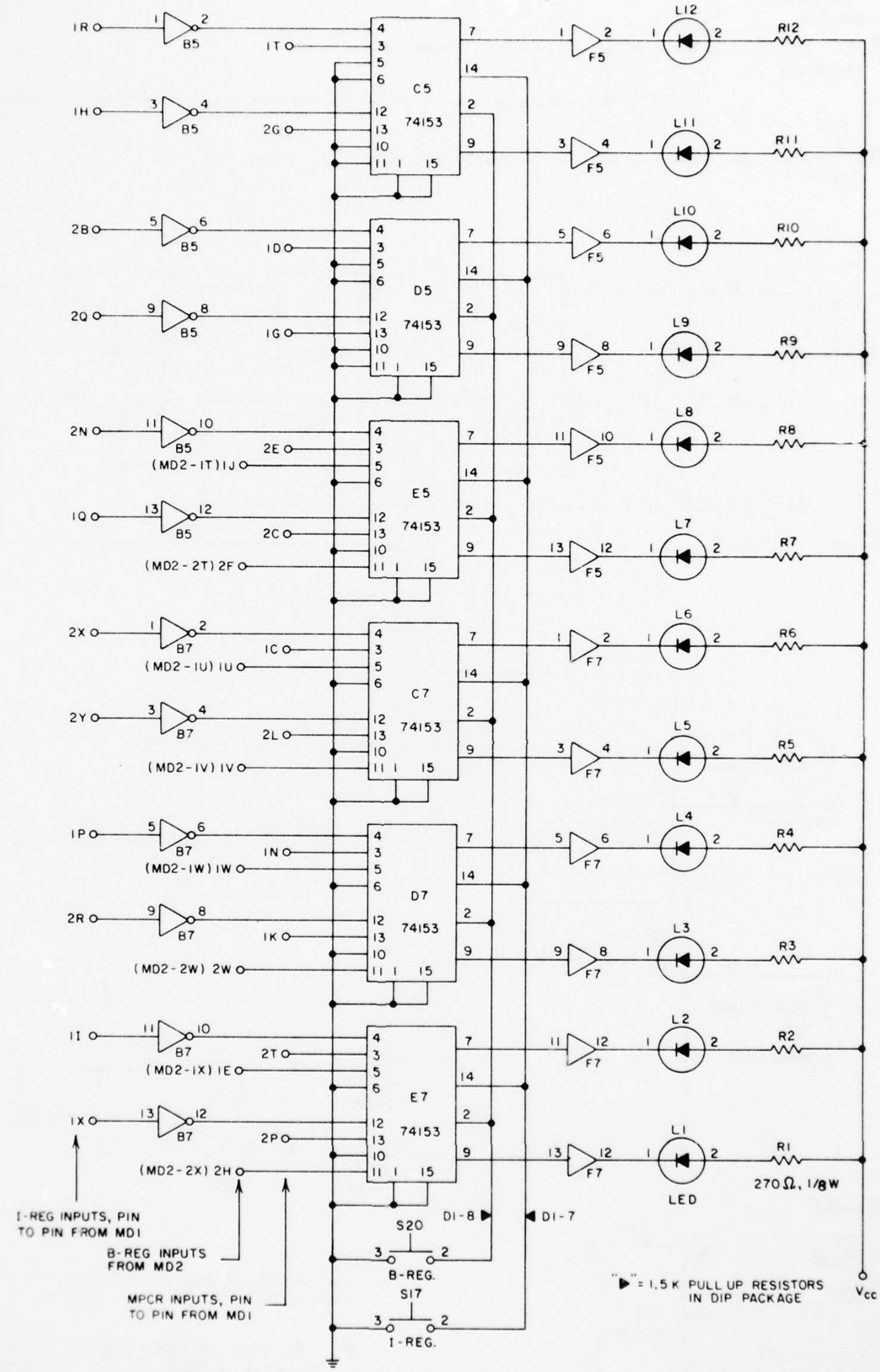


Figure 5-42. Monitor Board, Logic Diagram (Sheet 2 of 3)

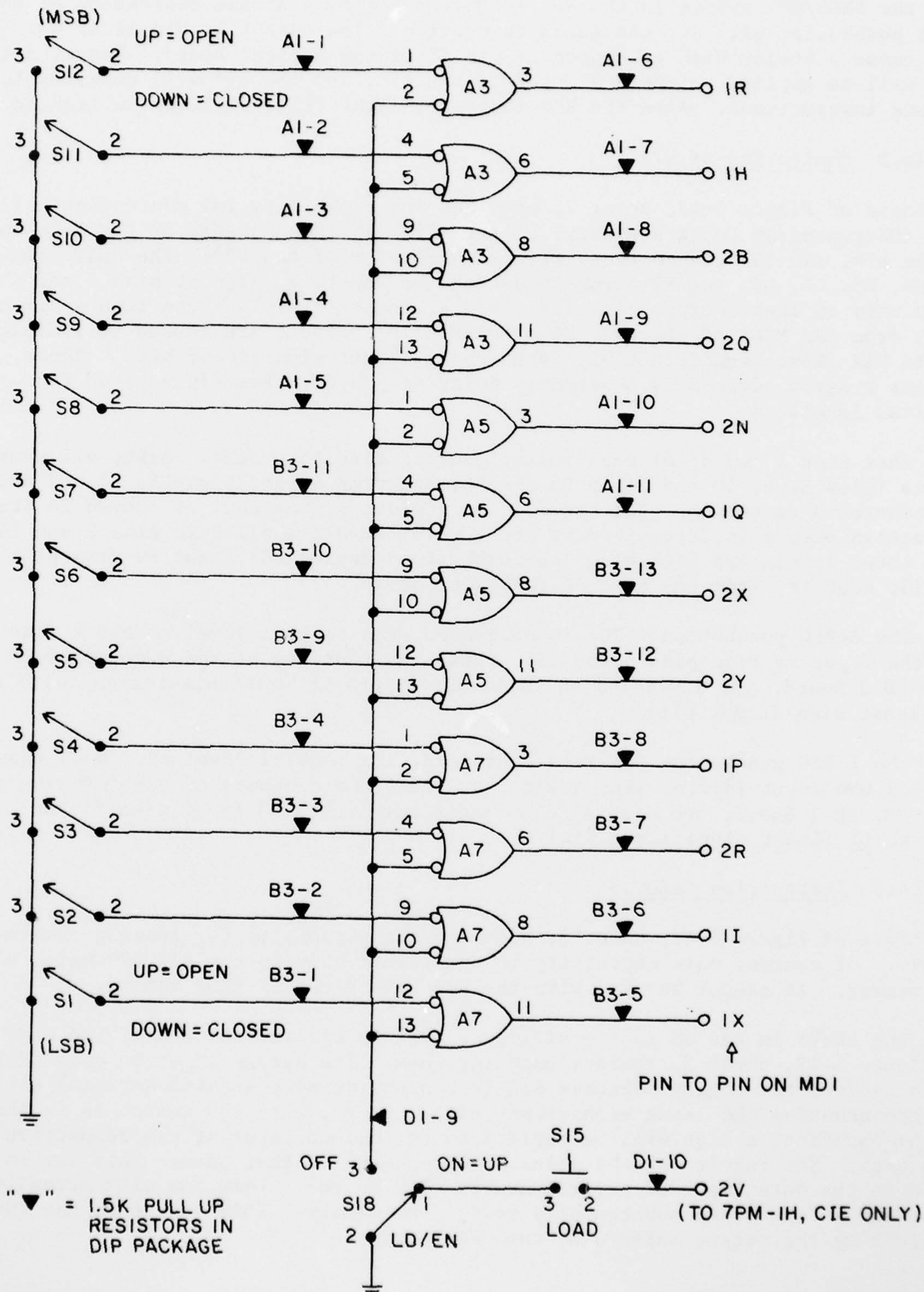


Figure 5-42. Monitor Board, Logic Diagram (Sheet 3 of 3)

With the SNGL/RUN switch in the RUN (down) position, a single depression of the START pushbutton will set the latch to provide a low output at pin 11 of C3. This will cause a steady high to appear at pin 1Y of the Monitor Board. Hence, a steady high will be applied to the RUN input of the B7*, and the B7* will continue to execute instructions. Also the RUN indicator light (L13) will remain lighted.

5.2.14.2 Monitoring of B7*

The logic of Figure 5-42, sheet 2, provides the capability for monitoring: (1) The MPCR (Microprogram Count Register) of the B7*, (2) the contents of the I-Register of the B7*, and (3) the contents of the B-Register of the B7*. The multiplexers C5, D5, E5, C7, D7, and E7 normally accept the inputs applied at pins 3 and 13 and route them to their outputs at pins 7 and 9, respectively. These inputs are normally from the MPCR of the B7*, MD 1 Board. The outputs are routed to indicator lights L12 (most significant bit) through L1 (least significant bit). Hence, the current program address is constantly being displayed. See Figure 5-43 for physical locations.

Note that pins 1 and 15 of each multiplexer is tied to ground. Also, all unused inputs (pins 5, 6, 10 and 11 on C5 and D5, and pins 6 and 10 on E5, C7, D7 and E7) are connected to ground. The specific multiplexer input that is routed to its respective output is determined by the control levels applied to pins 2 and 14. When these levels are both high (no pushbuttons depressed) input is from pins 3 and 13; that is, from the MPCR as indicated above.

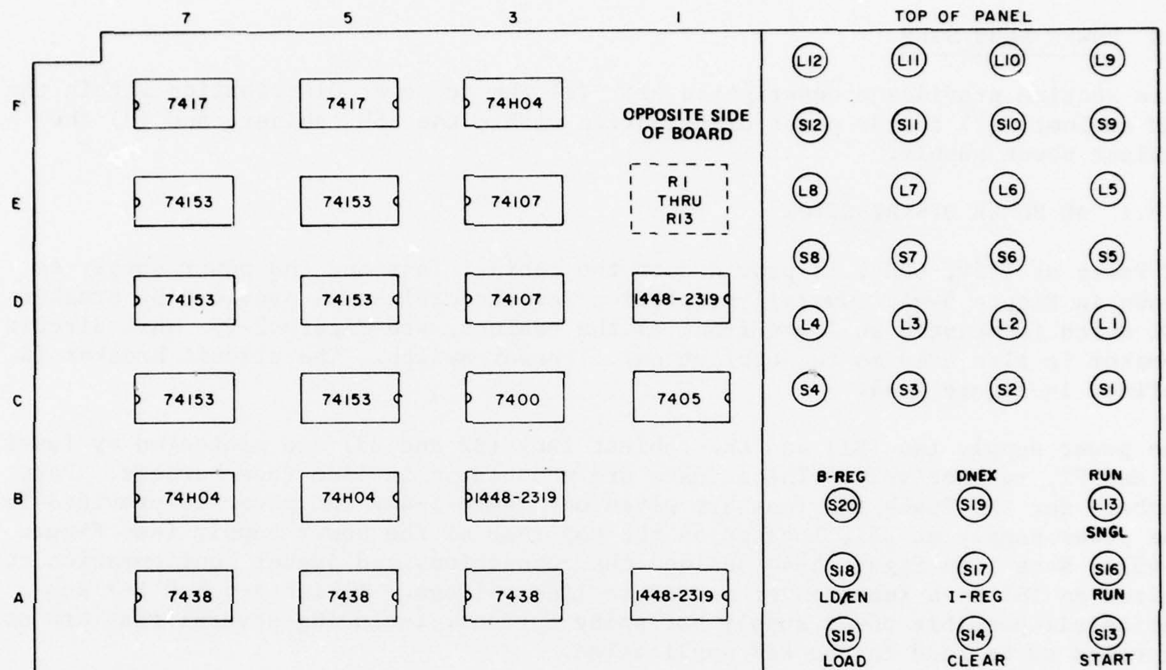
When the B-REG pushbutton (S20) is depressed, the control level at pin 2 goes low and the input is from pins 5 and 11. Thus, the contents of the B-register on the B7*, MD 2 Board, are displayed on indicator lights L8 (most significant bit) through L1 (least significant bit).

When the I-REG pushbutton (S17) is depressed, the control level at pin 14 goes low and the input is from pins 4 and 12. Thus, the contents of the I-Register on the B7*, MD 1 Board, are displayed on indicator lights L8 (most significant bit) through L1 (least significant bit).

5.2.14.3 Instruction Loading

The logic of Figure 5-42, sheet 3, provides the capability for loading program memory. Of course, this capability is applicable only to the CIE B7* which has RAM memory. It cannot be used with the NCU B7* which has PROM memory.

With the LD/EN in the ON (up) position, a high is applied to each of the NAND gates of Figure 5-42, sheet 3, thereby enabling them. The second input to each of these gates is from the toggle switches S12 (representing most significant bit) through S1 (representing the least significant bit). Hence, when any switch is in the up (open) position, a high will be applied to the second input of the respective NAND gate. The result will be a low of the output of that gate. This low is applied to the data input of program memory (7PM Board). This low will actually represent a "one" when subsequently ready from memory. This is due to the inversion provided by the output buffers on the 7PM Board.



IDENT	LOCATION
7400	C3
74404	B5, B7, F3
7405	C1
7417	F5, F7
7438	A3, A5, A7
74107	D3, E3
74153	C5, C7, D5, D7, E5, E7
BURROUGHS	1448-2319 RESISTOR DIP, BOARD LOCATIONS A1, B3, D1

IDENT	LOCATION
S13, S14, S15, S17, S20	SWITCH, PUSH BUTTON, C&K NO. 81213
S1 THRU S12, S19, S18	SWITCH, SPDT, C&K NO. 7101 SYZQ
S16	SWITCH, DPDT, C&K NO. 7201 SYZQ
L1 THRU L13	LIGHT, LED, DIALCO NO. 521-9167
R1 THRU R13	RESISTOR, 270 OHM, 1/8W, 5% TOL.

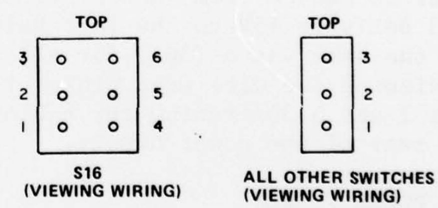


Figure 5-43. Monitor Board, Parts Layout Diagram and Parts List

With the toggle switches set (up = 1, down = 0) to represent the specific instruction to be loaded, the LOAD pushbutton must be momentarily depressed. This provides a momentary low signal at output pin 2V of the Monitor Board. This pulse is routed (via backplane wiring) to the "write pulse" input (pin 2V) on the Program Memory (7PM) Boards. There it strobes the states (instruction) set by the toggle switches into the program memory location indicated by lights L12 through L1.

5.3 POWER SUBSYSTEM

This section provides a description of: (1) The ac power distribution within the ESM cabinet, (2) the dc power distribution within the ESM cabinet, and (3) the cabinet power supply.

5.3.1 AC POWER DISTRIBUTION

AC Power at 115V, 60Hz, is provided to the cabinet fans and the power supply as shown in Figure 5-44. Overall protection for the cabinet is provided by breaker CB1 which is mounted at lower front of the cabinet, see Figure 2-2. This circuit breaker is also used as the cabinet on/off power switch. The circuit breaker is defined in Figure 5-44.

The power supply fan (B1) and the cabinet fans (B2 and B3) are protected by fuses F1 and F2, respectively. These fuses are mounted in in-line fuse holders. Part numbers for the fuses and fans are given on Figure 5-44. AC power is provided to the power supply at TB1, located on the top rear of the power supply (see Figure 5-45). Note 1 on Figure 5-44 defines the connections and jumber configuration required on TB1 as a function of actual ac line voltage. Tables 5-6 and 5-7 summarize all possible power supply strapping options, including several that are not expected to be used in the ESM application.

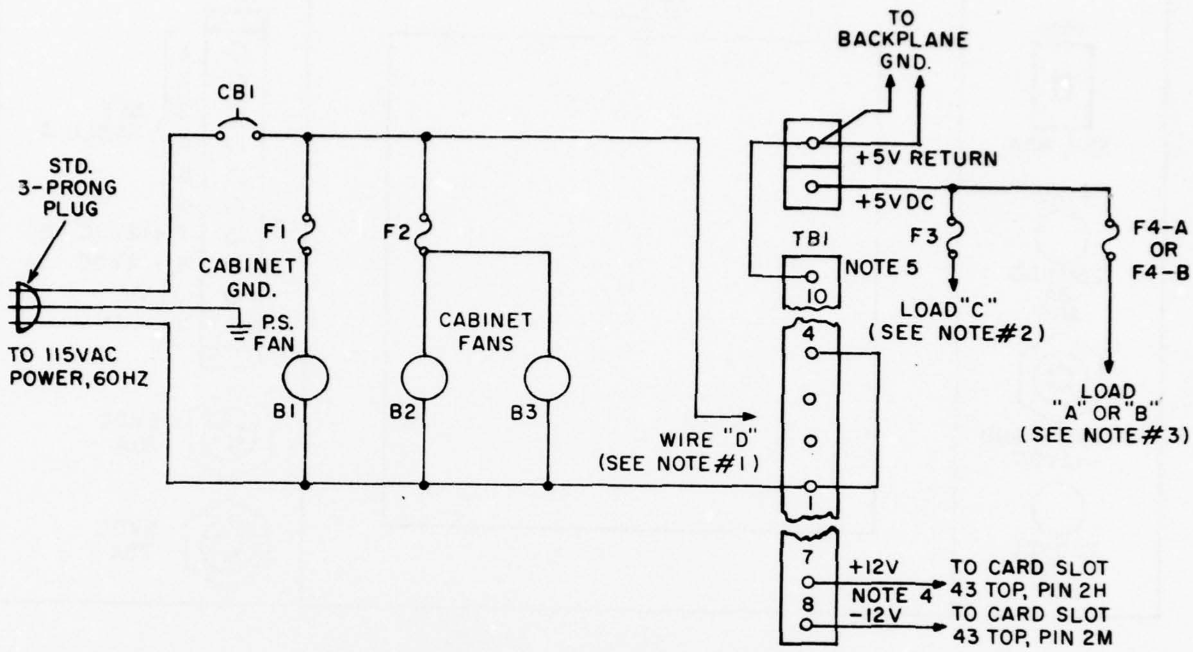
5.3.2 DC POWER DISTRIBUTION

DC Power distribution is provided for +5 Volts in all cabinets. In addition distribution is provided for +12 Volts and -12 Volts in cabinet 3, only.

DC Power is routed from the +5V terminal of the power supply via two separate fuses. Fuse F3 delivers +5V to the left half (viewing the wire wrap pins) of the backplane, and is the same value (30A) for all cabinets. Fuse F4 delivers +5V to the right half (viewing the wire wrap pins) of the backplane. This fuse has a 15A rating for cabinet 1 and a 30A rating for cabinets 2 and 3. These fuses are mounted in clips at the rear of the power supply.

5.3.3 POWER SUPPLY

The Power Supply (Burroughs Part Number 1742-7394) has a +5V current rating of 75A, and a +5V regulation of $\pm 3\%$. It also delivers +12V at 1.5 amps and -12V at 0.5A. Regulation at +12V and -12V is $\pm 10\%$. Ripple is 50 millivolts (maximum) for the +5V output and 200 millivolts (maximum) for the +12V and -12V outputs.



SYMBOL	PART NO.	DESCRIPTION	RATING
CB1	AIRPAX UPL1-515-63	CIRCUIT BREAKER	15 AMP, 250 VAC, 60 HZ, MOTOR START
F1, F2	3AG	FUSE	1/2 AMP, 250 VOLT
B1, B2, B3	ROTRON MARK 4	FAN	115 VAC, 14 WATT
F3	5AG	FUSE FOR +5 VDC, LOAD "C"	30 AMP, 32 VOLT
F4-A	5AG	FUSE FOR +5 VDC, LOAD "A"	15 AMP, 32 VOLT
F4-B	5AG	FUSE FOR +5 VDC, LOAD "B"	30 AMP, 32 VOLT

NOTES:

1. FOR LINE VOLTAGE OF 120-130 VAC ATTACH WIRE "D" TO TB1-3 & ADD JUMPER, TB1-3 TO TB1-6. FOR LINE VOLTAGE OF 110-120 VAC ATTACH WIRE "D" TO TB1-2 & ADD JUMPER, TB1-2 TO TB1-5.
2. LOAD "C" COVERS ALL PC CARDS TO THE LEFT (VIEWING WIRE-WRAP PINS) OF THE CLOCK CARD.
3. LOAD "A" & "B" COVER THE CLOCK CARD AND ALL PC CARDS TO ITS' RIGHT (VIEWING WIRE-WRAP PINS). LOAD "A" APPLIES ONLY TO LOOP #1. LOAD "B" APPLIES ONLY TO LOOPS #2 & #3.
4. +12V & -12V OUTPUT ARE USED ONLY IN CABINET #3.
5. TB1-9 & 10 ARE THE RETURN SIDES OF THE +5 VOLT, +12 VOLT, AND -12 VOLT SUPPLIES.

Figure 5-44. AC and DC Power Distribution

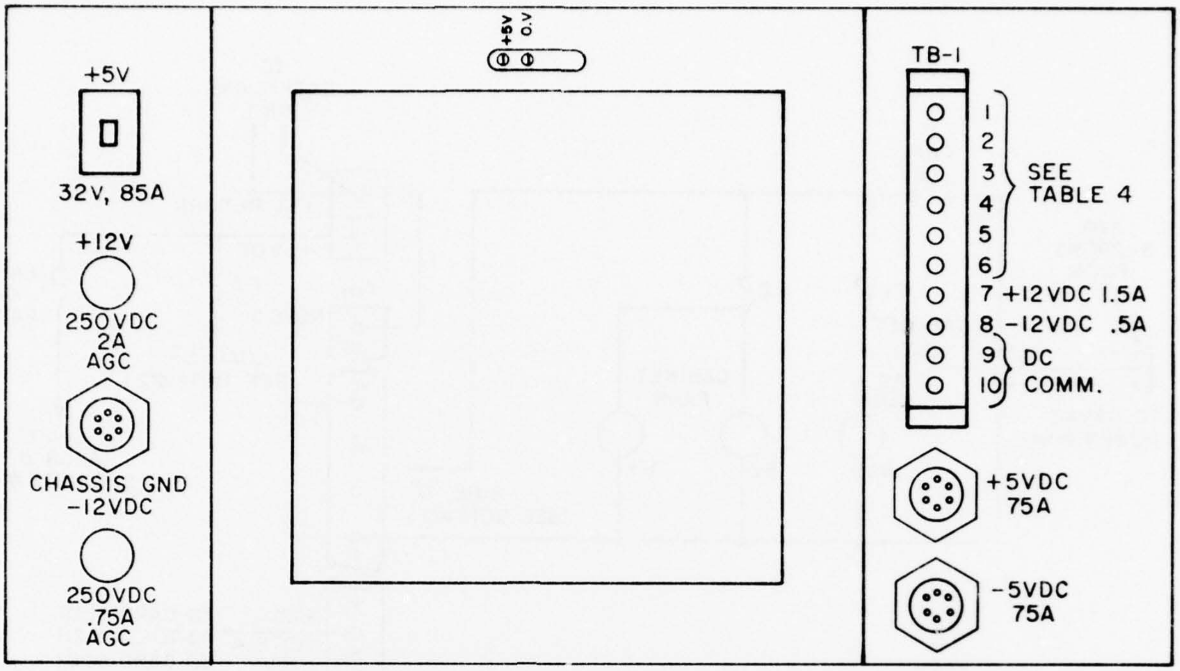


Figure 5-45. Power Supply - Top View

As installed in the ESM cabinets, the power supply is intended for operation from ac line voltages of 110V to 130V, when strapped in accordance with note 1 of Figure 5-44. Input voltage tolerance should be +6%, -10%. Frequency should be 60 Hz ± 1%. The power supply is equipped with a cooling fan for normal operation and is equipped with an automatically resetting thermal cut-out that interrupts operation if safe operating temperature is exceeded. See Table 5-8.

The AC input to the power supply is protected by the external circuit breaker shown in Figure 5-44. The +5V supply is protected by the circuit breaker mounted at the top front of the supply, Figures 5-45 and 5-46. The +12V and -12V outputs are protected by fuses also mounted at the top front of the supply, Figures 5-45 and 5-46.

Overvoltage protection limits the +5V output to 25% overvoltage by means of a crowbar circuit which grounds the output. Overcurrent protection is also incorporated in the +5V output and is immediately activated if the output is shorted to ground. When the short circuit is removed, normal operation automatically resumes.

The complete schematic for the power supply is presented in figure 5-46, sheets 1 and 2.

The +5 volt output can be continuously adjusted ±5%, minimum, from nominal voltage. This adjustment is accessible from the top of the supply, see Figure 5-45. This adjustment is further described in the following paragraph.

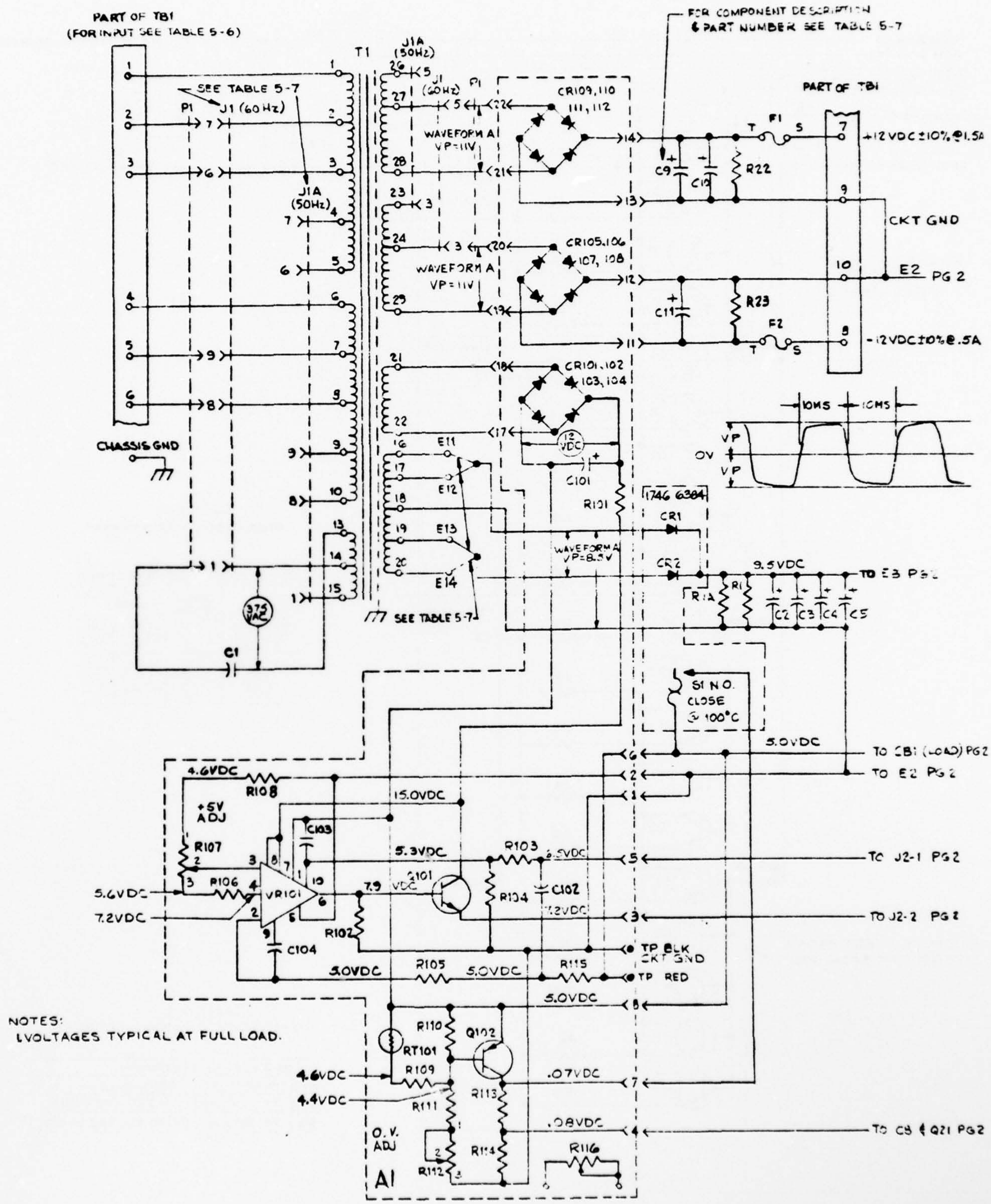


Figure 5-46. Power Supply Subsystem, Power Distribution Diagram (Sheet 1 of 2)

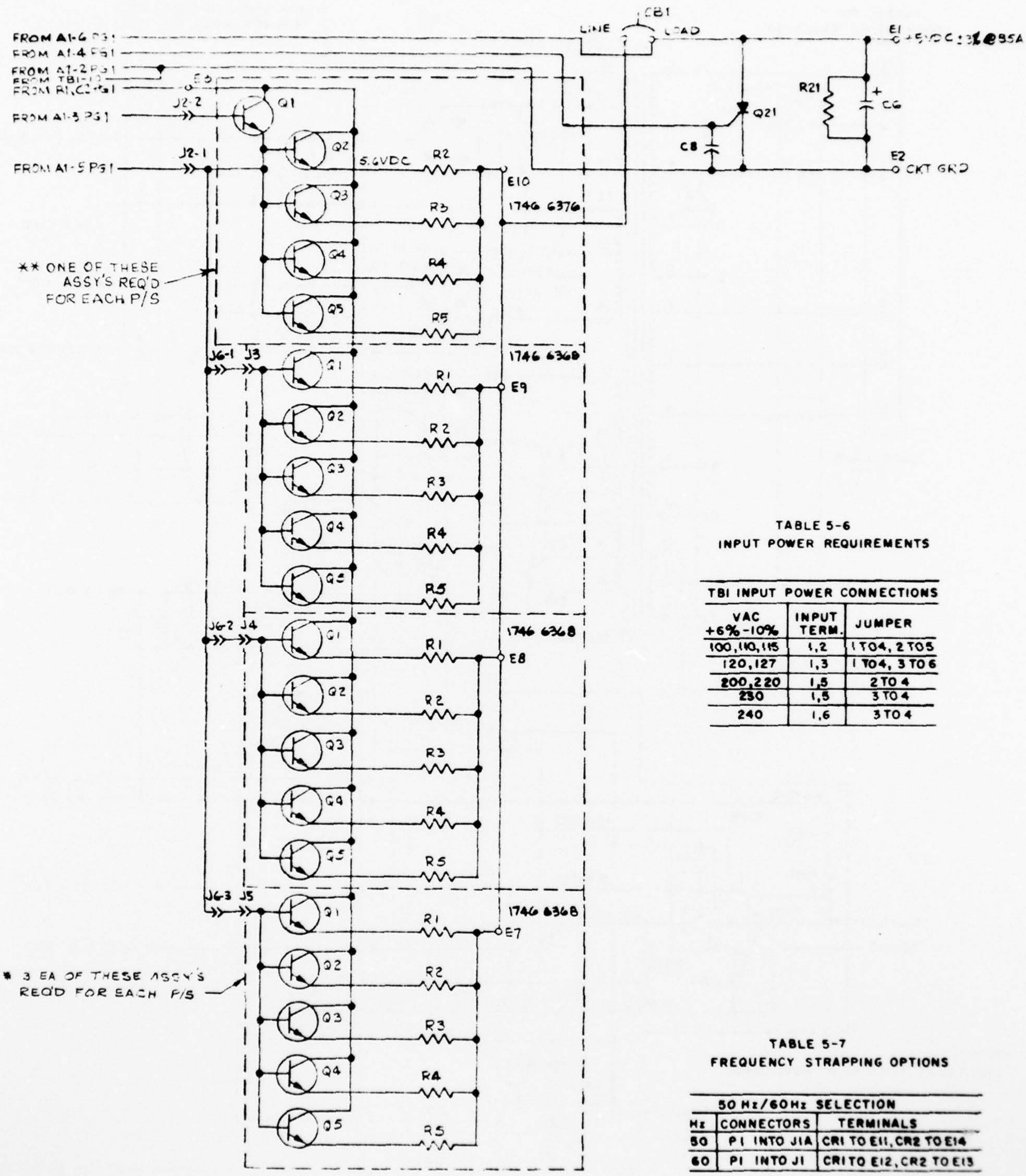


TABLE 5-6
INPUT POWER REQUIREMENTS

TBI INPUT POWER CONNECTIONS		
VAC +6% -10%	INPUT TERM.	JUMPER
100,110,115	1,2	1 TO 4, 2 TO 5
120,127	1,3	1 TO 4, 3 TO 6
200,220	1,5	2 TO 4
230	1,5	3 TO 4
240	1,6	3 TO 4

TABLE 5-7
FREQUENCY STRAPPING OPTIONS

50 Hz/60Hz SELECTION		
Hz	CONNECTORS	TERMINALS
50	P1 INTO J1A	CR1 TO E11, CR2 TO E14
60	P1 INTO J1	CR1 TO E12, CR2 TO E13

Figure 5-46. Power Supply Subsystem, Power Distribution Diagram (Sheet 2 of 2)

Table 5-8. Power Supply Parts List

Reference Designation	Description	Part No.
A1	Printed Wiring Board	1746 6392
CB1	Circuit Breaker, 85A. 32VDC	2600 3780
CR1, CR2	Diode, 70A, 200 PIV	1742 7832
CR101-CR104	Diode, 1N645	1745 1360
CR105-CR108	Diode, 1A. 400 PIV	1745 1378
CR109-CR112	Diode, 1N4719	1119 4800
C1	Capacitor, 15 uf, 660VDC	2601 1783
C2, C5	Capacitor, 185,000 uf, 15VDC	1734 6552
C6	Capacitor, 18,000 uf, 10VDC	1734 6586
C7	Not Used	
C8	Capacitor, 1 uf, 35VDC	1267 9031
C9-C11	Capacitor, 36,000 uf, 15VDC	1734 6578
C101	Capacitor, 500 uf, 15V	1742 7782
C102	Capacitor, .0047 uf, 100V	1745 1329
C103	Capacitor, .0022 uf, 100V	1745 1337
C104	Capacitor, 680 pf, 100V	1716 8907
F1	Fuse, 2A., 250V, AGC	1321 8631
F2	Fuse, .75A., 250V, AGC	1343 0921
*	Heat Sink Assembly	1746 6368
Q1-Q5	Transistor	2600 3798
R1-R5	Resistor, .1 ohm, ±1%, 3W	1742 8129
**	Heat Sink Assembly	1746 6376
Q1-Q5	Transistor	2600 3798
R2-R5	Resistor, .1 ohm, ±1%, 3W	1742 8129

Table 5-8. Power Supply Parts List (Cont)

Reference Designation	Description	Part No.
Q21	SCR C52U	1745 1303
Q101	Transistor 2N3767	1745 1386
Q102	Transistor 2N3133	1742 7857
RT101	Thermistor	1742 8160
R1, R1A	Resistor, 5 ohms, ±5%, 50W	1742 7931
R21	Resistor, 24 ohms, ±5%, 2W	1265 8357
R22	Resistor, 80 ohms, ±10%, 3W	1742 3137
R23	Resistor, 240 ohms, ±5%, 2W	1265 9074
R101	Resistor, 20 ohms, ±5%, 2W	1265 8290
R102	Resistor, 3K ohms, ±2%, 1/2W	1114 9366
R103	Resistor, 243 ohms, ±1%, 1/2W	1742 9523
R104	Resistor, 1.1K ohms, ±1%, 1/2W	1742 8020
R105	Resistor, 1500 ohms, ±1%, 1/2W	1110 3944
R106	Resisotr, 750 ohms, ±1%, 1/2W	1114 8798
R107	Resistor, Variable, 500 ohms, ±10%, 1W	1719 4002
R108	Resistor, 2.21K ohms, ±10%, 1/2W	1742 9515
R109	Resistor, 425 ohms, ±10%, 1/2W	1742 7972
R110	Resistor, 225 ohms, ±10%, 1/2W	1742 7980
R111	Resistor, 500 ohms, ±10%, 1/2W	1742 8004
R112, R116	Resistor, Variable, 2K ohms, ±10%, .75W	1719 4028
R113	Resistor, 10 ohms, ±2%, 1/2W	1268 7414
R114	Resistor, 510 ohms, ±2%, 1/2W	1100 3910
R115	Resistor, 100 ohms, ±2%, 1/2W	1100 3720

Table 5-8. Power Supply Parts List (Cont)

Reference Designation	Description	Part No.
S1	Thermostat, close @ 100°C	1745 1311
T1	Transformer	1742 8202
VR101	Regulator, UA723C	1729 7284

5.3.4 CABINET POWER SUPPLY (5VDC) CHECKS

1. Frequency of Check: Semiannually or whenever components are replaced in the supply.

2. Equipment Required:

   Voltage Tests: One DC Digital Voltmeter

   Ripple Test: One Oscilloscope, 100 MV/CM minimum vertical sensitivity

   Tools: One pocket or jewelers screwdriver

3. Preliminary Conditions: Verify that all PC Boards, front plane connector blocks and interconnecting cables between PC Boards are installed. Turn on cabinet power and allow a 15 minute warmup period.

4. Measurement Location: Take all V_{CC} measurements on backplane wire-wrap pins between the specified V_{CC} (see Note) and backplane ground. The +12V and -12V supplies may be measured at TB1-7 and TB1-8, respectively, using TB1-10 as the return.

5. Ripple Test: Verify that the ripple between any V_{CC} terminal and ground is 150 MV peak-to-peak or less before proceeding. Verify that the ripples on the +12V and -12V supplies on cabinet 3 are 400 MV peak-to-peak or less before proceeding. Note that the ripple figures specified in paragraph 5.3.3 are for new equipment without consideration of component aging.

6. Voltage Balance: Measure the DC voltage on any V_{CC} pin to the right of the clock card and compare it to the voltage on any V_{CC} pin to the left of the clock card. If the difference is greater than 0.150 VDC the problem should be corrected before proceeding. No adjustment is available but a high resistance wire connection or a shorted PC Card would be likely causes.

7. Voltage Adjustment: Turn the "5VDC ADJ", if required, until the average of the two V_{CC} readings taken above is between 4.95 and 5.05 VDC.

8. Verify that the +12V and -12V levels are within 10% of 12V. There are no adjustments for the +12V and -12V power supplies.

NOTE

V_{cc} (5VDC) for each PC Card is located on the left-hand column (viewed from wire-wrap side of backplane) of wire-wrap pins, terminals "A" and "Z".

5.4 CABLING DEFINITION

This section defines the interconnecting cables between the ESM, CRT, and Host Processor, and includes the ESM inter-board cables and connector blocks.

Description	Cable or Connector Detail	Cable or Connector Installation
Frontplane Connector Block	Figure 5-47	Figure 2-4
Inter-Board Cables	Figure 5-48	Figure 2-4
Cable, ESM No. 1 to Host No. 1	Figure 5-49	Figure 2-1
Cable, ESM No. 2 to Host No. 2	Figure 5-50	Figure 2-1
Cable, ESM No. 1 to ESM No. 2	Figure 5-51	Figure 2-1
Cable, ESM No. 2 to ESM No. 3	Figure 5-52	Figure 2-1
Cable, ESM No. 3 to ESM No. 1	Figure 5-53	Figure 2-1
Cable, ESM No. 2 or 3 to CRT (TD 802)	Figure 5-54	Figure 2-1

5.5 SUMMARY OF CABINET CONFIGURATION

The ESM cabinets are standard Burroughs Corp. cabinets of the type used for the Burroughs B 711-2 Processor. The cabinet is equipped with its standard backplane and card rack, caster assembly, rear panel, side panels and top cover. It also includes the front panel (a glass door), part number 1448-9264, and cabinet fans. This is the same type of fan (Rotron Mark 4) that is mounted on the power supply.

The cabinet is also equipped with a cabinet ac circuit breaker/on-off switch. It is specifically identified in Figure 5-44 and its cabinet location is shown in Figure 2-2.

A separate panel containing switches, employed for maintenance and loading purposes, is also mounted on the cabinet per Figure 2-2. The panel contains one pushbutton switch and either 12 (for cabinet No. 1) or 14 (for cabinets No. 2 and No. 3) toggle switches. Identification of these switches is detailed in Figure 4-1 of the User Manual. Part numbers of the switches are as follows:

Pushbutton Switch	C & K 8121 Z
Toggle Switches	C & K 7101 SYZQ

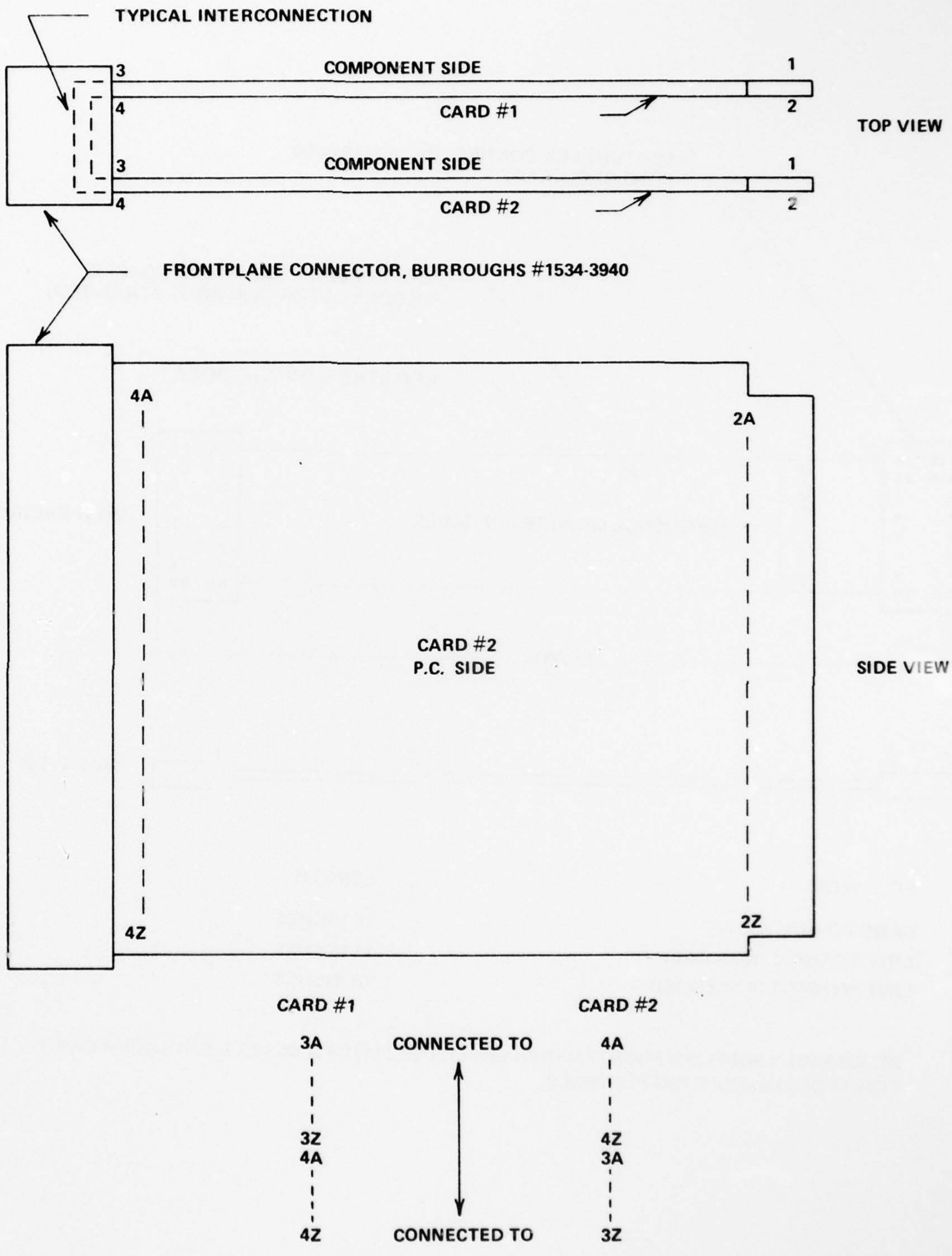


Figure 5-47. Frontplane Connector Block

AD-A063 370 BURROUGHS CORP PAOLI PA FEDERAL AND SPECIAL SYSTEMS GROUP F/G 17/2
EXPLORATORY SYSTEMS CONTROL MODEL (ESM). MAINTENANCE MANUAL.(U)
APR 77 DCA100-75-C-0054
UNCLASSIFIED SBIE-AD-E100 145 NL

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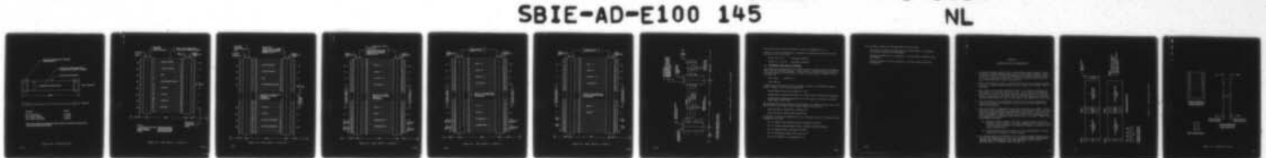

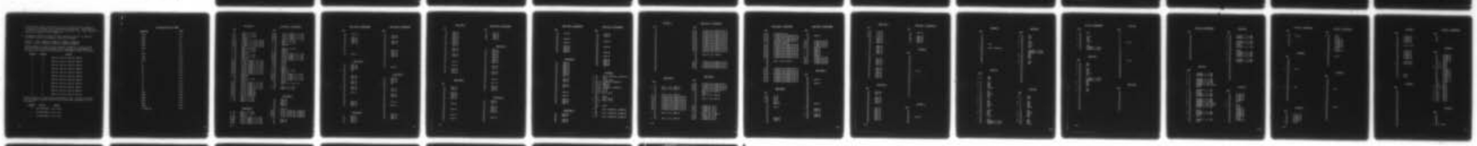

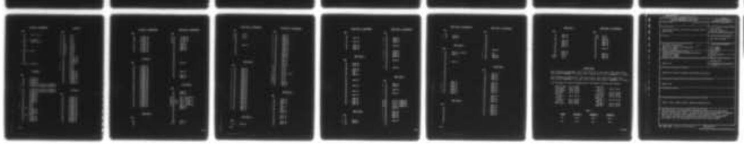

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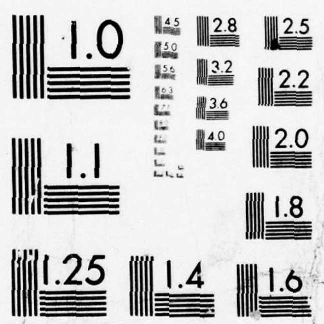
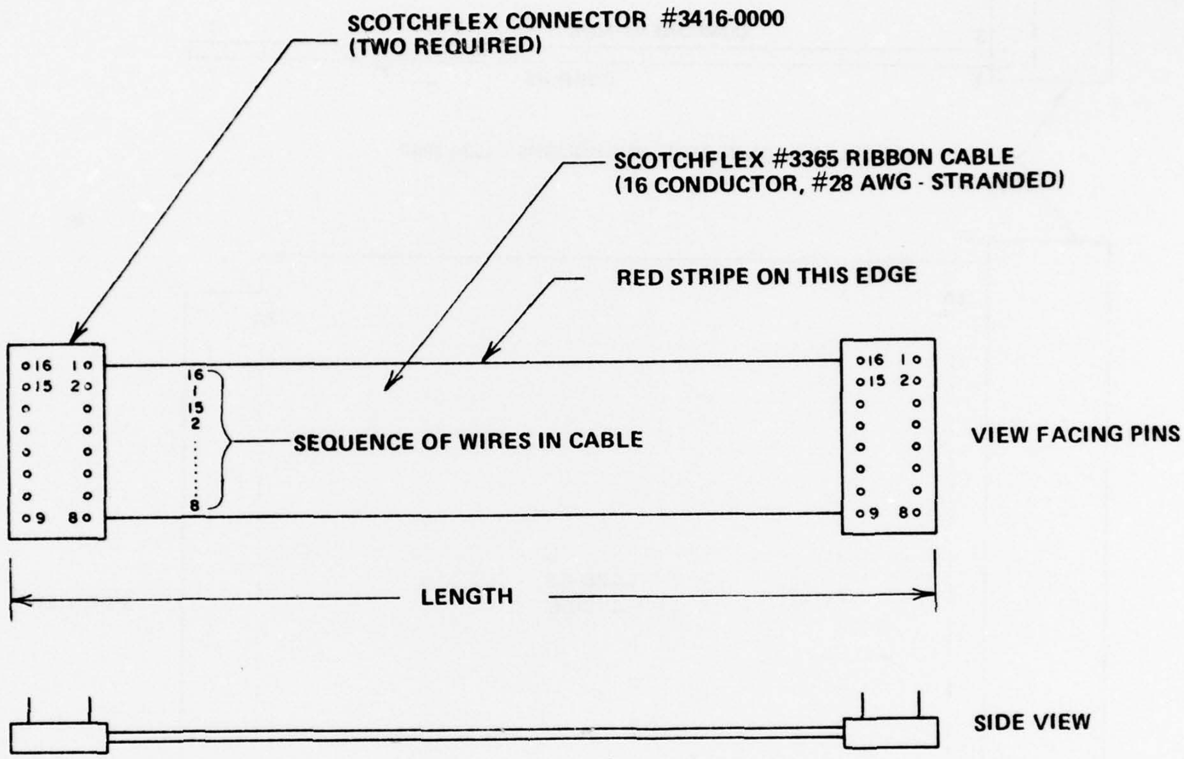


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A



LOCATION	LENGTH
CANC TO IH/IC/IA/IB	15 INCHES
LINT TO NMD1 (NORMAL)	11 INCHES
LINT TO NMD1 (EXTENDED*)	18 INCHES

*SEPARATELY SUPPLIED MAINTENANCE CABLE USED WITH A DOUBLE EXTENDER CARD FOR TROUBLESHOOTING PURPOSES.

Figure 5-48. Inter-Board Cables

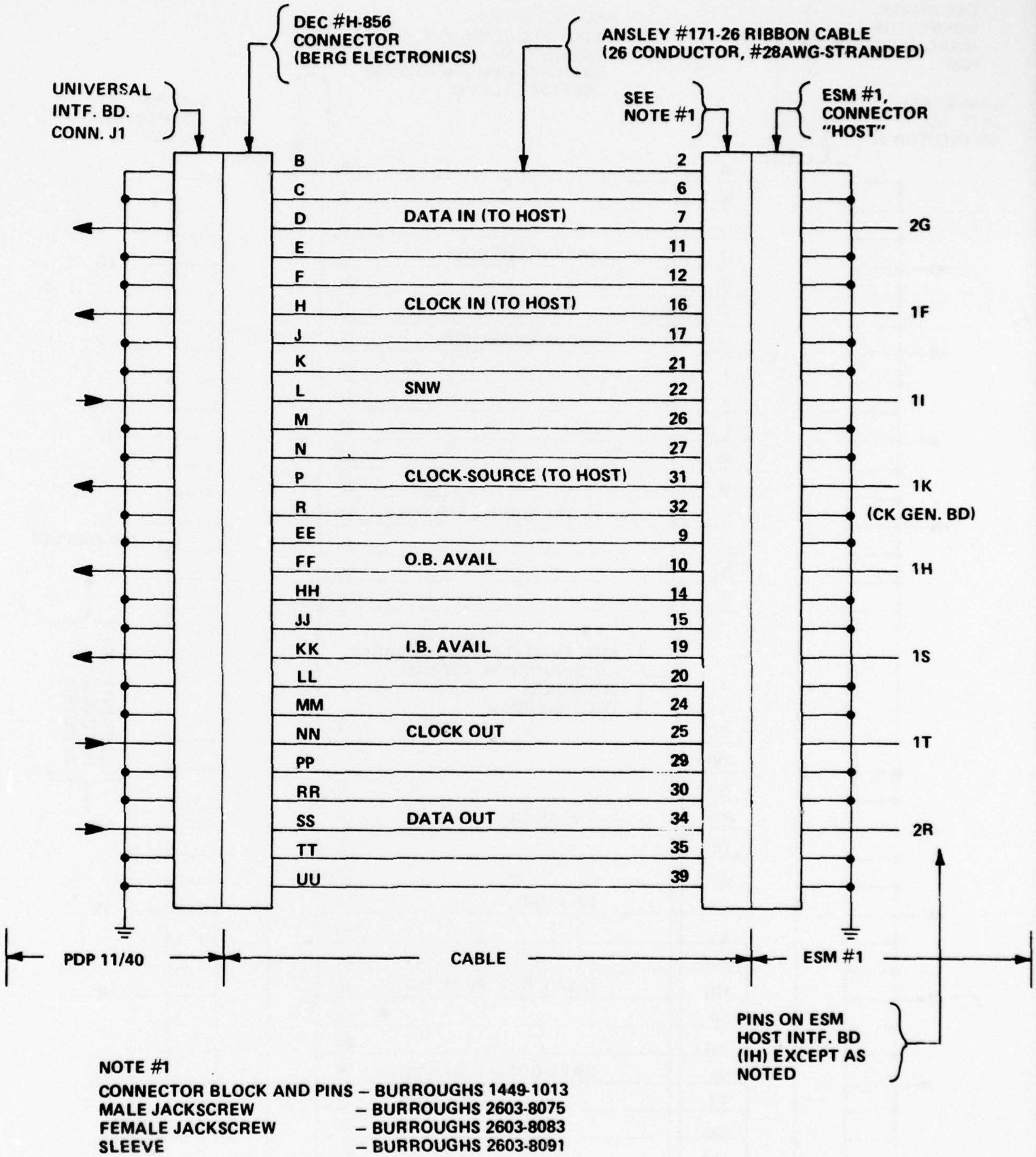


Figure 5-49. Cable, ESM No. 1 to Host No. 1

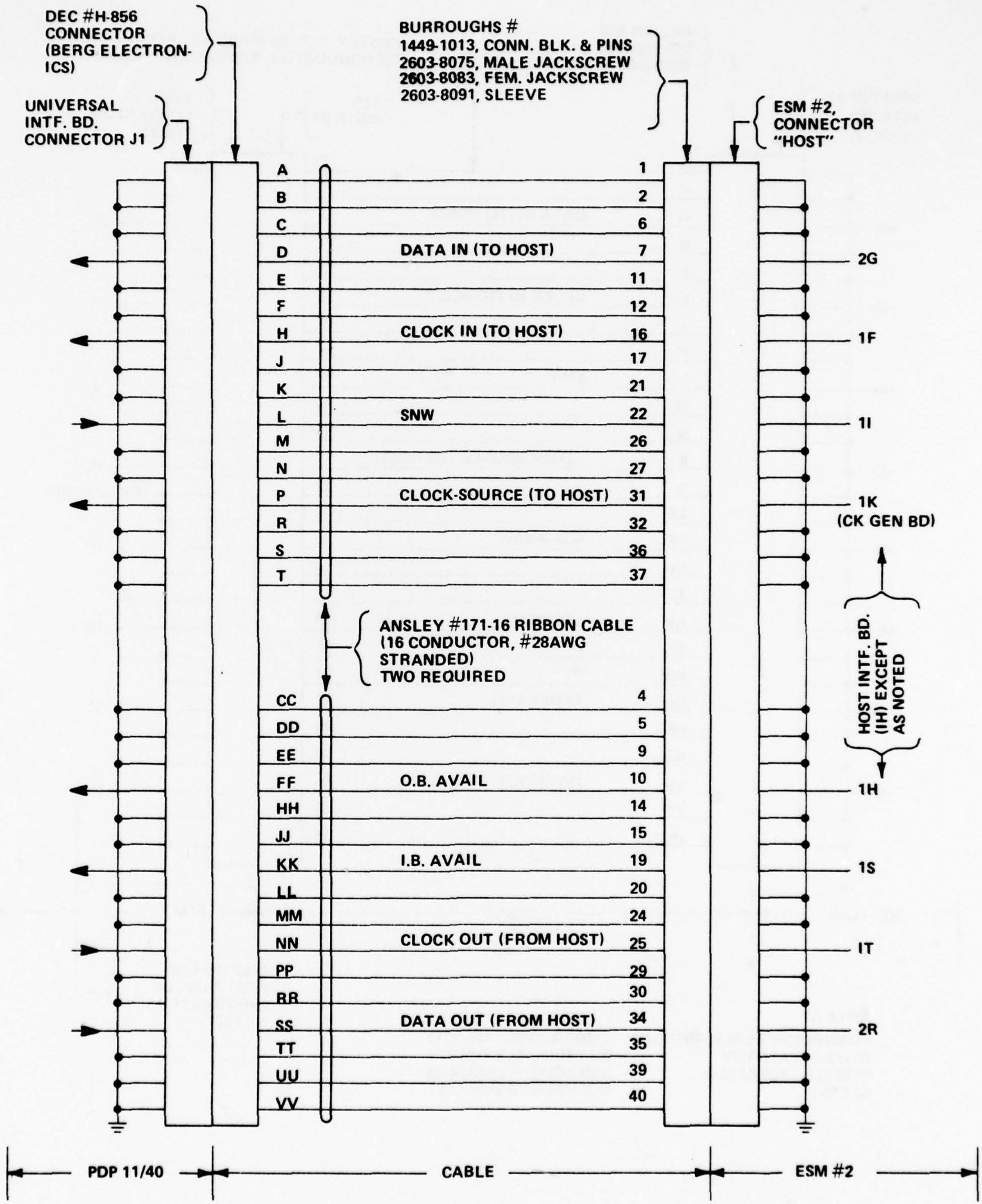


Figure 5-50. Cable, ESM No. 2 to Host No. 2

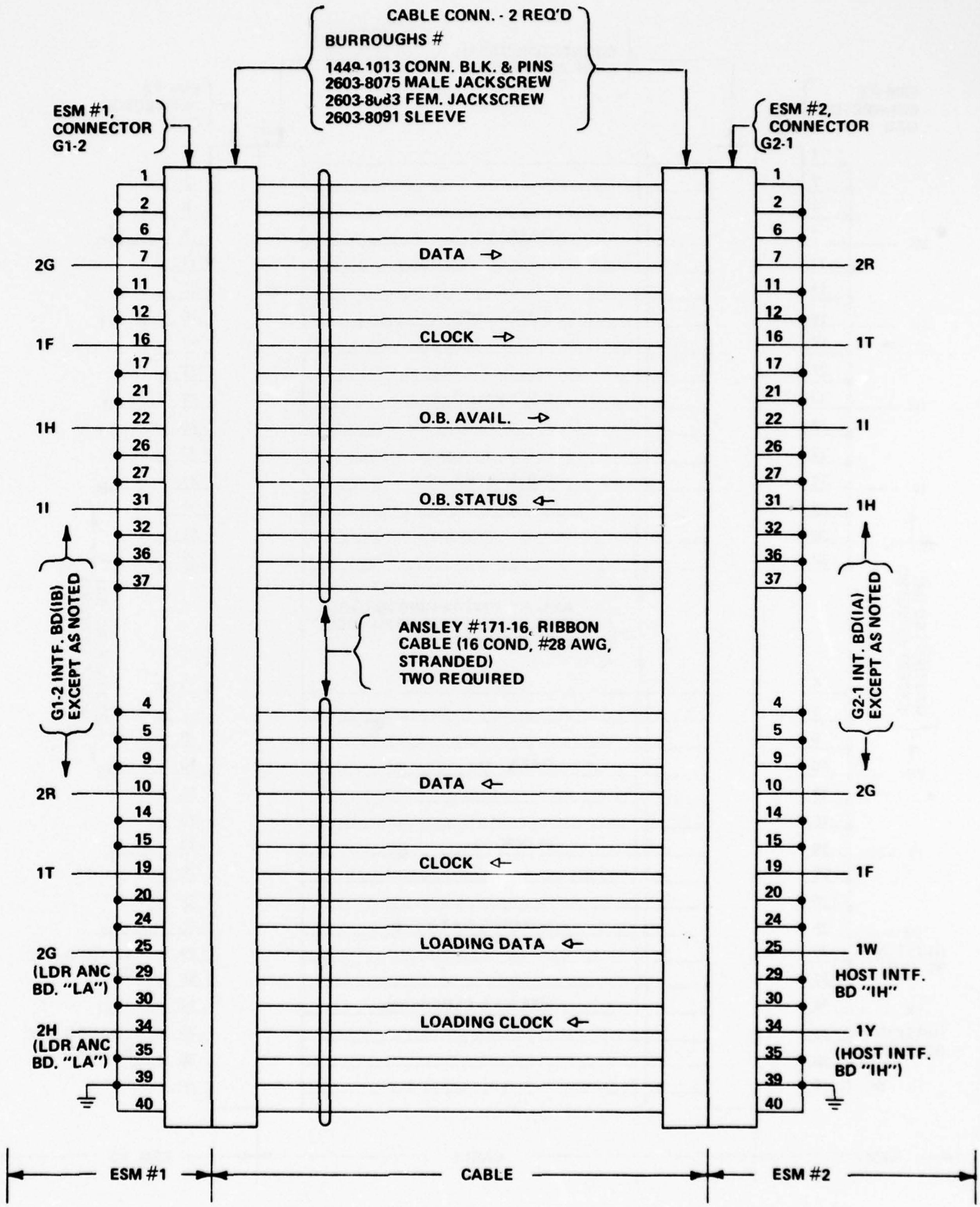


Figure 5-51. Cable, ESM No. 1 to ESM No. 2

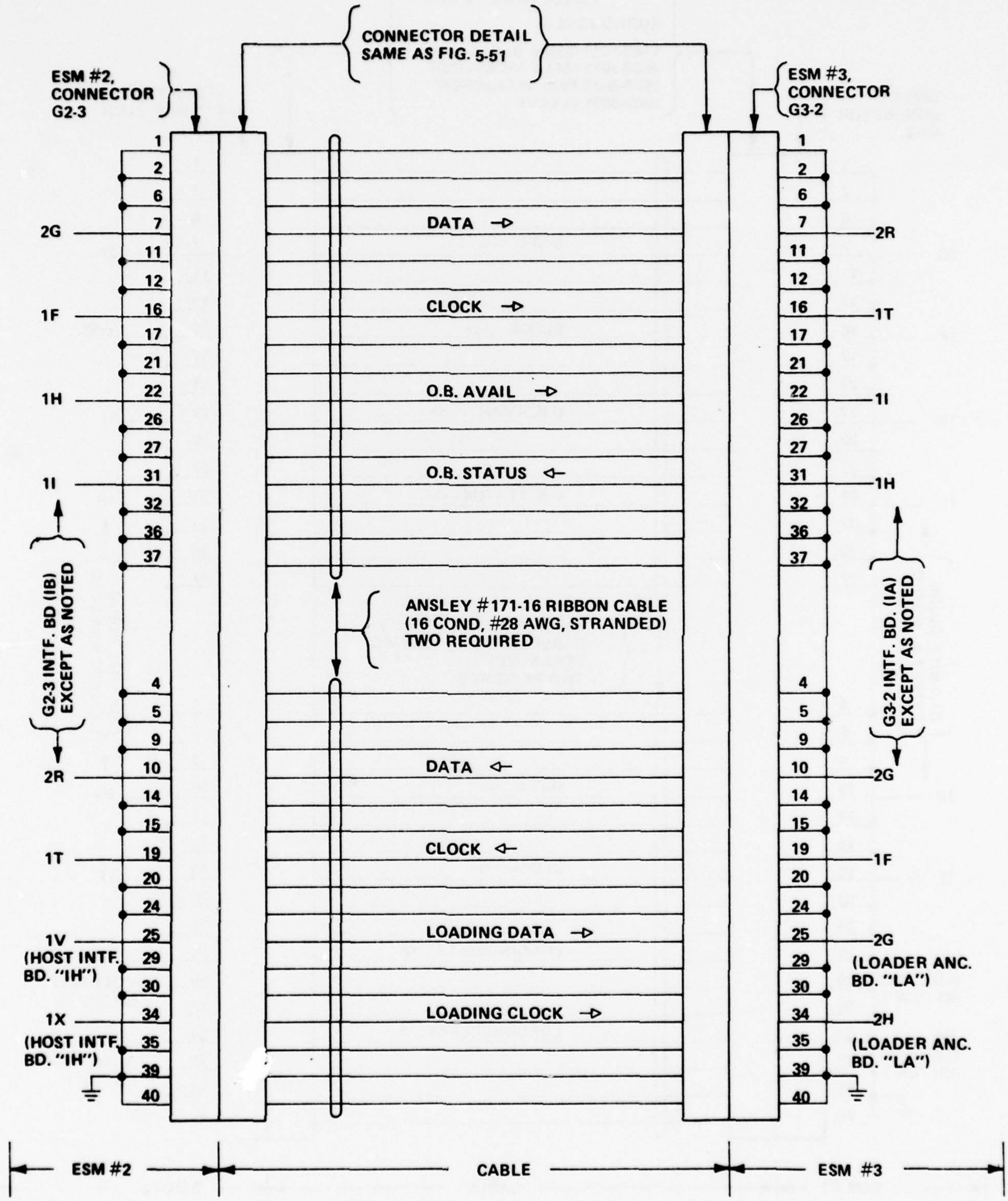


Figure 5-52. Cable, ESM No. 2 to ESM No. 3

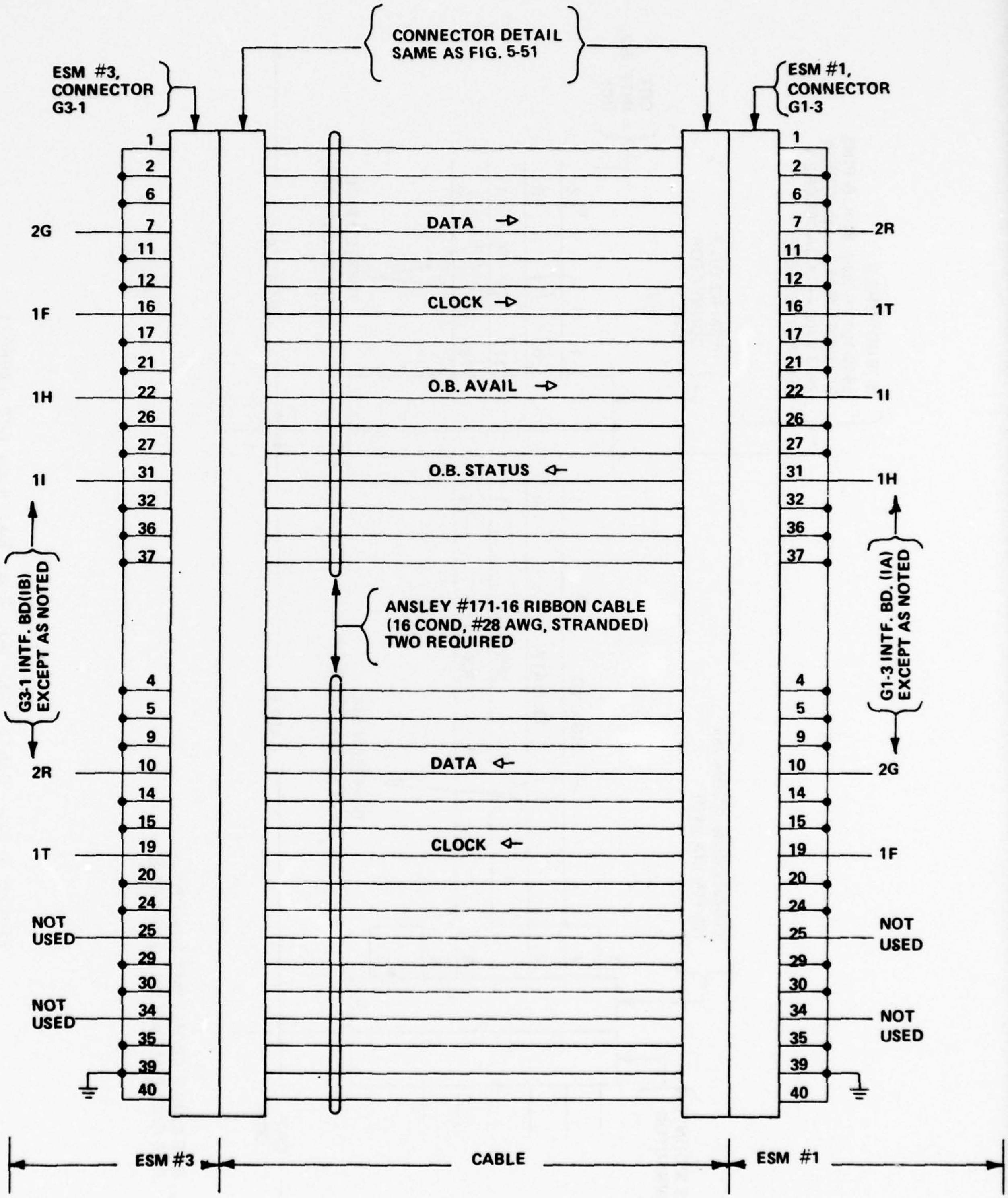


Figure 5-53. Cable, ESM No. 3 to ESM No. 1

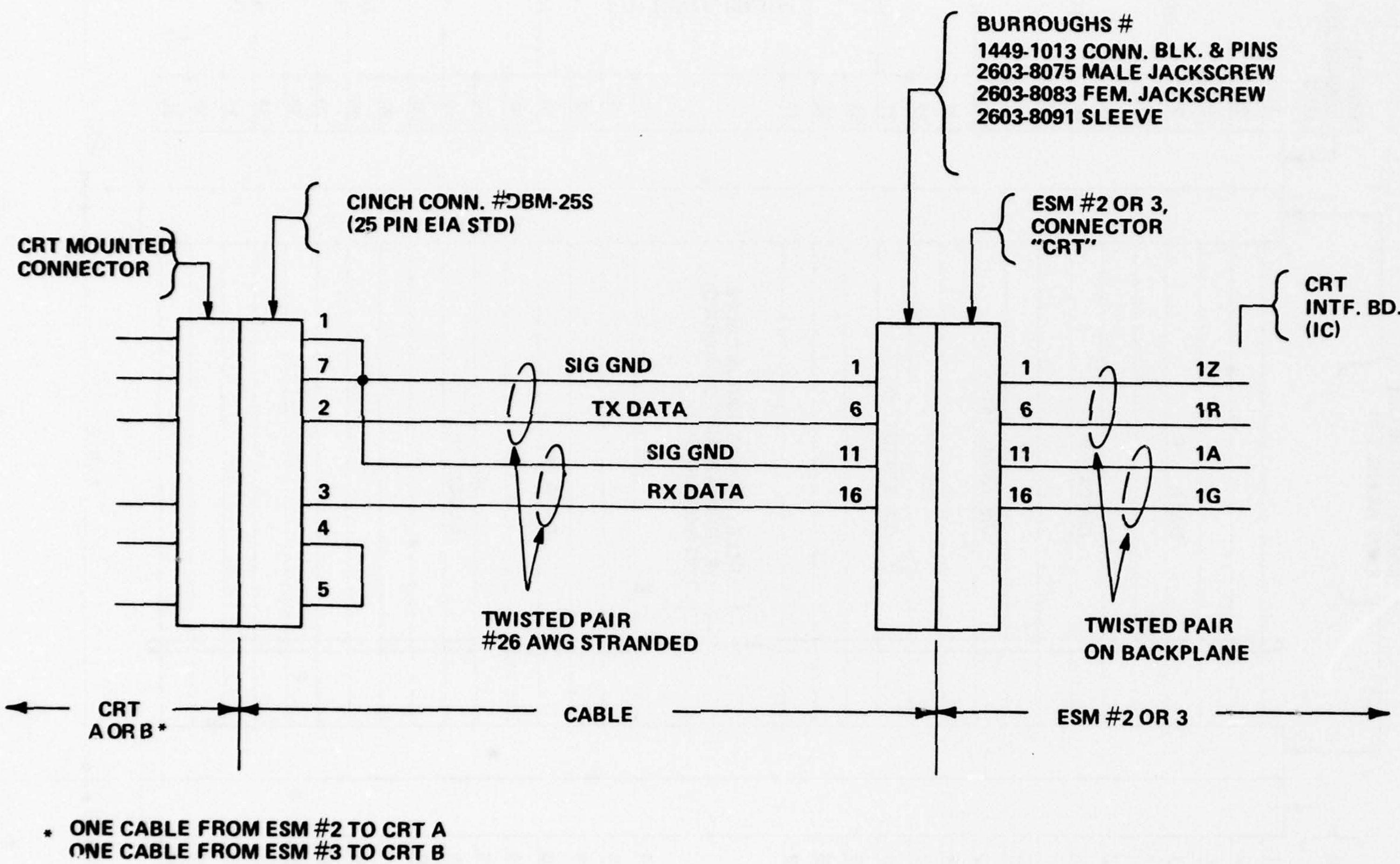


Figure 5-54. Cable, ESM No. 2 or No. 3 to CRT (TD802)

The cabinet power supply is described in detail in paragraph 5.3.3.

Cabinet air filters (removable for cleaning) are provided in the bottom of each cabinet and are of two types:

Filter (6" x 24")   Burroughs 1448-5494

Filter (6" x 17-3/4")   Burroughs 1449-1286

5.6 MAINTENANCE TOOLS AND TEST EQUIPMENT

Tools required for maintenance of the ESM include the standard types of electronic hand tools and soldering equipment. These include a chip puller and chip inserter for proper removal and installation of chips on the PC Boards. Typical tools of this type are:

Chip puller   AUGAT T114-1

Chip inserter

A wire-wrap gun and bits should be available to repair or reconfigure backplane wiring. Typical tools for this purpose are:

Gardner-Denver Wire Wrap Gun Model No. 14R2

Gardner-Denver Wrapping Bit/Sleeve for 26 AWG (used for ESM Cabinet Backplane)

Gardner-Denver Wrapping Bit/Sleeve for 30 AWG (used for Universal Interface Board added to PDP-11/40)

The following tools would facilitate replacement of the female connector pins on the PDP-11/40 end of the "ESM to Host" cables, Figures 5-49 and 5-50:

Berg Electronics, Model HT-95, Crimping Tool

Berg Electronics, Model HT-80, Removal Tool

In addition to the above standard tools, the following tools and a B7* Monitor were supplied with the ESM:

Two (2) Single Length Extender Boards, Burroughs 1447-9026

One (1) Double Length Extender Board, Burroughs 1447-9026 Modified

One (1) Extender Cable, Burroughs 1447-7822

Two (2) Maintenance Cables, see Figure 5-48

One (1) B7* Monitor, see paragraph 5.2.14

Test equipment required for ESM maintenance should include:

Oscilloscope, 50 MHz, with Dual Trace and Delayed Sweep - for Waveform Monitoring and Pulse Width Measurement

Multimeter, Simpson 260, or equivalent - for resistance and signal level measurements

Digital Voltmeter, .01 Volt resolution - for Power Supply checks and adjustments

APPENDIX A

BACKPLANE WIRE LIST INTERPRETATION

1. The backplane wiring consists only of intra-cabinet circuits between PC board connectors, external interface connectors and control panel switches. Refer to Figure A-1 for the location and labeling of the cabinet sections and Figure A-2 for the orientation of the pins. Frontplane connector blocks and inter-board ribbon cables are covered in Section 5-4.

2. Within the listing, all pins on a given horizontal line are connected together. There are no interconnections between lines or between left and right sides of the pages.

3. Each circuit has one master reference location in the listing, identified by the presence of an asterisk (*) on that line. All pins are cross referenced back to this location. The master reference location lists all of the connections in a given circuit and shows which cabinets and sections are applicable. Erroneous conclusions will occur in many cases if this master line is not used.

4. The entire listing is in alpha-numeric order of the connector designations, using the headings for the connector title and the left hand column for the pins on that connector.

5. Node card connector designations contain four characters (e.g., CMD1). Unique connectors within the cabinet are designated by two characters (e.g., LD) except for switch designations S10 through S15 which contain three. Each master reference line implies a separate circuit for each node card designation, unless that designation is prefixed by a node letter (A, B, C, H) (e.g., H-CMD1), with the following exceptions.

   (1) Whenever a unique connector is listed it has the effect of tying all implied circuits together. The unique connection may be located in the left hand column, related to the connector heading, or anywhere on the master reference line.

   (2) The entire CRT node (C) of Cabinet 1 is not wired although the implication from the listing is to the contrary.

6. All listings apply to all cabinets (1, 2, 3) unless the master reference line restricts the applicability to one or more cabinets by adding cabinet numbers following the pin designation in the left hand column (e.g., "*1F,2,3 NANC-2S" which is at connector title "CK-SIDE 1").

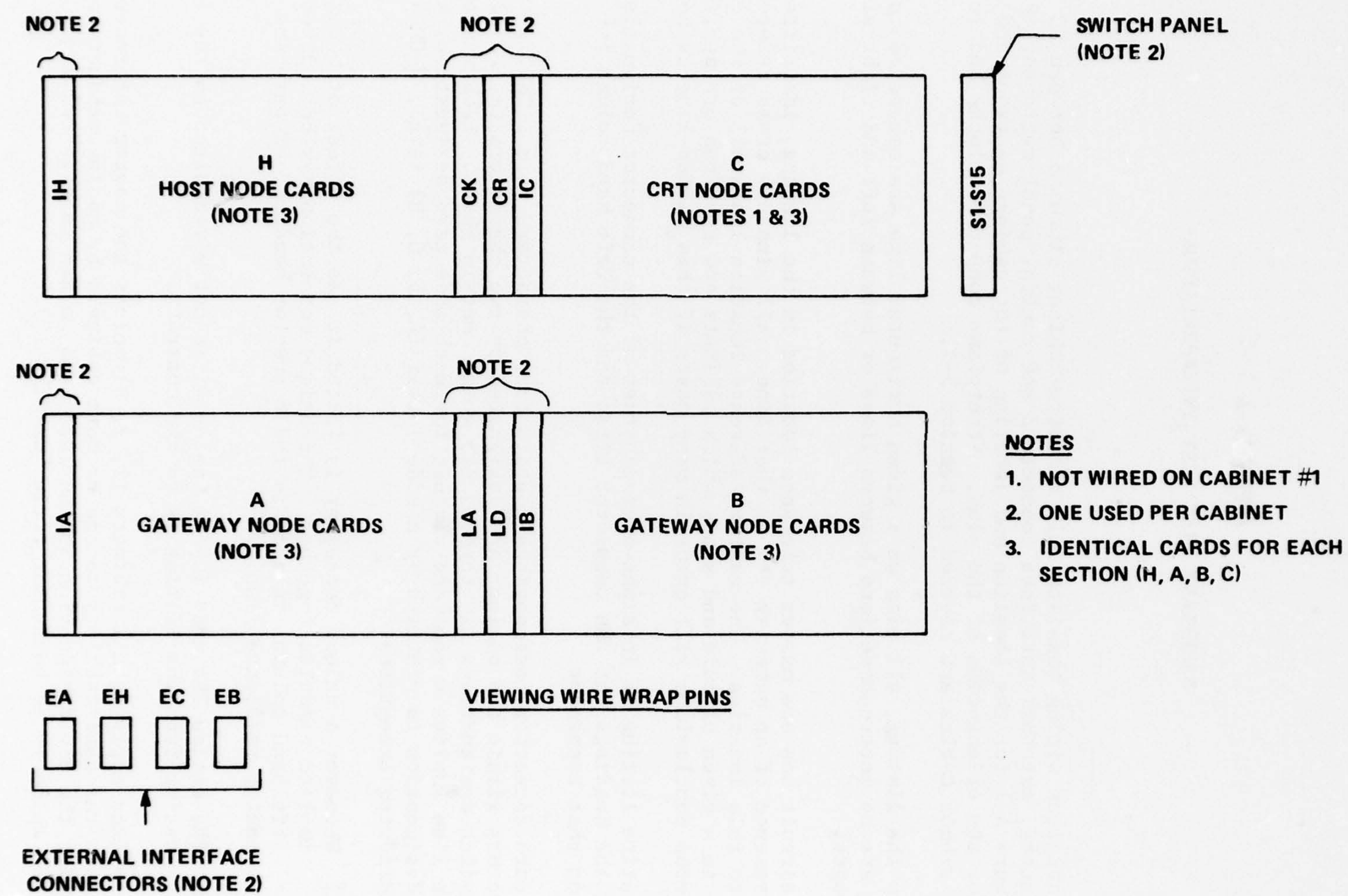


Figure A-1. Cabinet Wiring Sections

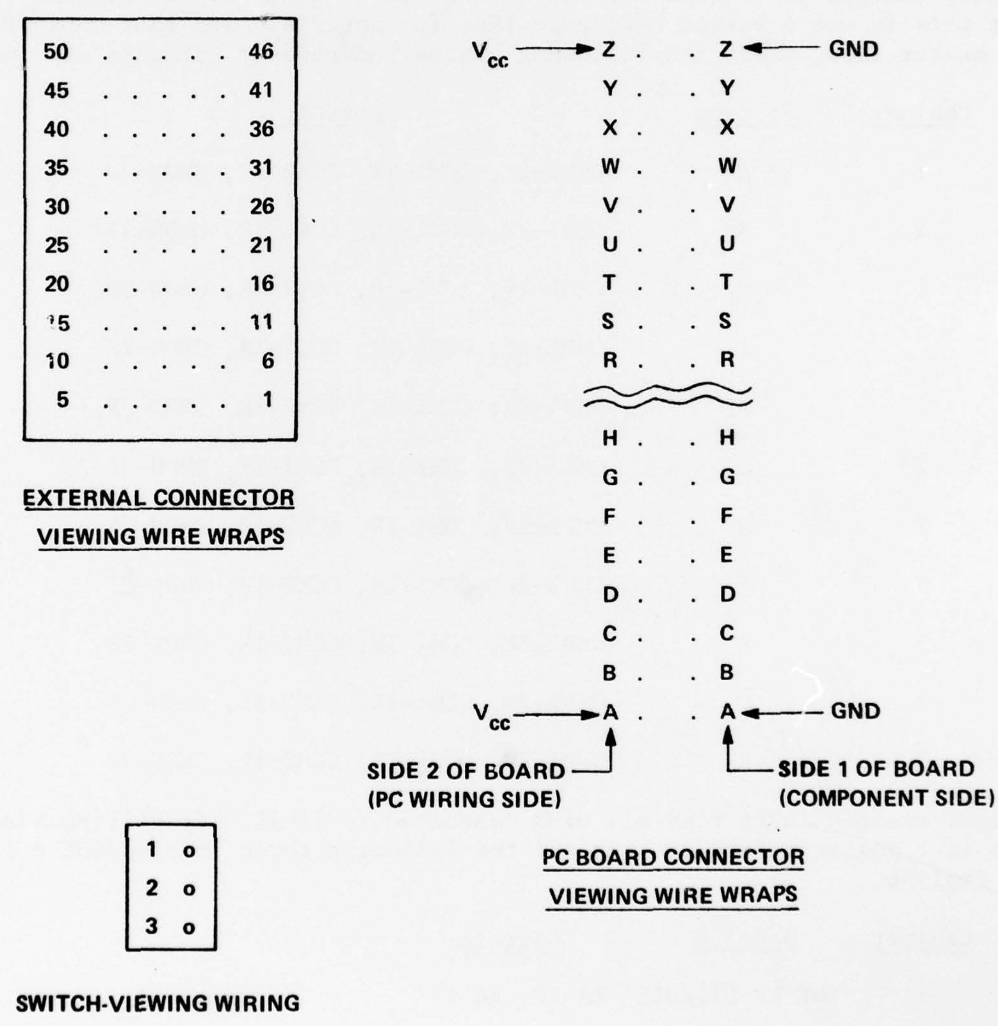


Figure A-2. Orientation of Pins

7. In cases where twisted pair wires are used, the notation "TW-G" is added to indicate that the signal wire is twisted with a ground wire. The ground wire is connected to ground at both ends of the twisted pair (e.g., "*1R TWG, EC-6" which is at connector title "IC-SIDE 1").

8. An example of using the listing is master reference line "1F" at connector "CK-SIDE 1" where the following two circuits are implied:

Cabinet 2 CK-1F, A-NANC-2S, B-NANC-2S, C-NANC-2S, H-NANC-2S
Cabinet 3 CK-1F, A-NANC-2S, B-NANC-2S, C-NANC-2S, H-NANC-2S

Another example is to find all pins connected to CCM1-1R. It will be seen that this is not a master reference line (no asterisk) and that CMD1-2P is the master line, where the following eleven independent circuits are implied.

Cabinet	Section	Circuit
1	A	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
1	B	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
1	H	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
2	A	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
2	B	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
2	C	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
2	H	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
3	A	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
3	B	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
3	C	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P
3	H	CMD1-2P, CCM1-1R, CCM2-1R, CMON-2P

A final example is to find all pins connected to IA-1F. It will be seen that this is a master reference line and the following three independent circuits are implied.

Cabinet	Section	Circuit
1	NOT APPLICABLE	IA-1F, EA-19
2	NOT APPLICABLE	IA-1F, EA-19
3	NOT APPLICABLE	IA-1F, EA-19

BACKPLANE WIRE LIST INDEX

CANC-SIDE 1

PIN	
* 1B	CDM1 & 2 & 3-1B
* 1C	CDM1 & 2 & 3-1C
* 1D	CDM1 & 2 & 3-1D
* 1E	CDM1-1E
*A-1F	A-CDM1 & 2 & 3-1F, IA-1D
*B-1F	B-CDM1 & 2 & 3-1F, IB-1D
*C-1F	C-CDM1 & 2 & 3-1F, IC-1D
*H-1F	H-CDM1 & 2 & 3-1F, IH-1D
* 1G	CDM1 & 2 & 3-1G
* 1H	CDM1 & 2 & 3-1H
* 1I	CDM1 & 2 & 3-1I
* 1J	CMD2-2Q
* 1K	CDM1 & 2 & 3-1K
* 1L	CDM1 & 2 & 3-1L
* 1M	CMD2-2U
*A-1N	IA-1M, A-CDM1 & 2 & 3-1N
*B-1N	IB-1M, B-CDM1 & 2 & 3-1N
*C-1N	IC-1M, C-CDM1 & 2 & 3-1N
*H-1N	IH-1M, H-CDM1 & 2 & 3-1N
*A-1P	IA-1N, A-CDM1 & 2 & 3-1P
*B-1P	IB-1N, B-CDM1 & 2 & 3-1P
*C-1P	IC-1N, C-CDM1 & 2 & 3-1P
*H-1P	IH-1N, H-CDM1 & 2 & 3-1P
* 1Q	CMD2-2E
* 1R	CMD2-1P
* 1S	CDM1 & 2 & 3-1S
1T	CMD2-1S
*A-1U	IA-1K, A-CDM1 & 2 & 3-1U
*B-1U	IB-1K, B-CDM1 & 2 & 3-1U
*C-1U	IC-1K, C-CDM1 & 2 & 3-1U
*H-1U	IH-1K, H-CDM1 & 2 & 3-1U
*A-1V	IA-1J, A-CMD1-2D
*B-1V	IB-1J, B-CMD1-2D
*C-1V	IC-1J, C-CMD1-2D
*H-1V	IH-1J, H-CMD1-2D
* 1W	CDM1 & 2 & 3-1W
* 1X	CDM1 & 2 & 3-1X
* 1Y	CDM1 & 2 & 3-1Y

CANC-SIDE 2

* 2B	CDM1 & 2 & 3-2B
* 2C	CDM1 & 2 & 3-2C
* 2D	CMD2-1L
*A-2E	IA-1E, A-CDM1 & 2 & 3-2E
*B-2E	IB-1E, B-CDM1 & 2 & 3-2E
*C-2E	IC-1E, C-CDM1 & 2 & 3-2E
*H-2E	IH-1E, H-CDM1 & 2 & 3-2E

CANC-SIDE 2 (CONTINUED)

PIN	
*A-2F	IA-1C, A-CDM1 & 2 & 3-2F
*B-2F	IB-1C, B-CDM1 & 2 & 3-2F
*C-2F	IC-1C, C-CDM1 & 2 & 3-2F
*H-2F	IH-1C, H-CDM1 & 2 & 3-2F
* 2G	CDM1 & 2 & 3-2G
* 2H	CDM1 & 2 & 3-2H
* 2I	CDM2-1E
2J	
* 2K	CDM1 & 2 & 3-2K
* 2L	CDM3-1E
* 2M	LINT-1G
*A-2N	IA-1B, A-CDM1 & 2 & 3-2N
*B-2N	IB-1B, B-CDM1 & 2 & 3-2N
*C-2N	IC-1B, C-CDM1 & 2 & 3-2N
*H-2N	IH-1B, H-CDM1 & 2 & 3-2N
A-2P	LA-1H
B-2P	LA-1G
C-2P	LA-1F
H-2P	LA-1E
* 2Q	CMD2-2C
* 2R	CDM1 & 2 & 3-2R
* 2S	CMD2-1K
*A-2T	IA-1L, A-CDM1 & 2 & 3-2T
*B-2T	IB-1L, B-CDM1 & 2 & 3-2T
*C-2T	IC-1L, C-CDM1 & 2 & 3-2T
*H-2T	IH-1L, H-CDM1 & 2 & 3-2T
2U	IH-2K
* 2V	CDM1 & 2 & 3-2V & 2W
2W	
* 2X	CDM1 & 2 & 3-2X
* 2Y	CDM1 & 2 & 3-2Y

CCM1-SIDE 1

1B	CMD1-2X
1C	CMD1-2Y
1D	CMD1-2B
1E	CMD1-1Q
1F	
1G	CMD1-1T
*A-1H	LA-2L, A-CCM2-1H, A-CMON-2V
*B-1H	LA-2M, B-CCM2-1H, B-CMON-2V
*C-1H	LA-2K, C-CCM2-1H, C-CMON-2V
*H-1H	LA-2J, H-CCM2-1H, H-CMON-2V
1I	
1J	CMD1-2E
1K	CMD1-1C
1L	

CCM1-SIDE 1 (CONTINUED)

PIN	
1M	CMD1-1T
1N	
1P	CMD1-1N
1Q	CMD1-1D
1R	CMD1-2P
1S	CMD1-1K
1T	
1U	
1V	
1W	
1X	
1Y	CMD1-1I

CCM1-SIDE 2

PIN	
2B	CMD1-1H
2C	CMD1-2N
2D	CMD1-2Q
* 2E	VCC
2F	
2G	
2H	CMD1-1R
2I	CMD1-1G
2J	
2K	CMD1-2C
2L	CMD1-2G
2M	
* 2N	CCM2-1G
2P	CMD1-2L
2Q	
2R	CMD1-2T
2S	
2T	
2U	
2V	
2W	CMD1-2R
2X	CMD1-1P
2Y	CMD1-1X

CCM2-SIDE 1

PIN	
1B	CMD1-2X
1C	CMD1-2Y
1D	CMD1-2B
1E	CMD1-1Q

CCM2-SIDE 1 (CONTINUED)

PIN	
1F	
1G	CCM1-2N
1H	CCM1-1H
1I	
1J	CMD1-2E
1K	CMD1-1C
1L	
1M	
1N	
1P	CMD1-1N
1Q	CMD1-1D
1R	CMD1-2P
1S	CMD1-1K
1T	
1U	
1V	
1W	
1X	
1Y	CMD1-1I

CCM2-SIDE 2

PIN	
2B	CMD1-1H
2C	CMD1-2N
2D	CMD1-2Q
* 2E	VCC
2F	
2G	
2H	CMD1-1R
2I	CMD1-1G
2J	
2K	CMD1-2C
2L	CMD1-2G
2M	
2N	
2P	CMD1-2L
2Q	
2R	CMD1-2T
2S	
2T	
2U	
2V	
2W	CMD1-2R
2X	CMD1-1P
2Y	CMD1-1X

CDM1-SIDE 1

PIN	
1B	CANC-1B
1C	CANC-1C
1D	CANC-1D
1E	CANC-1E
1F	CANC-1F
1G	CANC-1G
1H	CANC-1H
1I	CANC-1I
1J	
1K	CANC-1K
1L	CANC-1L
1M	
1N	CANC-1N
1P	CANC-1P
1Q	
1R	
1S	CANC-1S
1T	
1U	CANC-1U
1V	
1W	CANC-1W
1X	CANC-1X
1Y	CANC-1Y

CDM1-SIDE 2

PIN	
2B	CANC-2B
2C	CANC-2C
2D	
2E	CANC-2E
2F	CANC-2F
2G	CANC-2G
2H	CANC-2H
2I	
2J	
2K	CANC-2K
2L	
2M	
2N	CANC-2N
2P	
2Q	
2R	CANC-2R
2S	
2T	CANC-2T
2U	

CDM1-SIDE 2 (CONTINUED)

PIN	
2V	CANC-2V
2W	CANC-2V
2X	CANC-2X
2Y	CANC-2Y

CDM2-SIDE 1

1B	CANC-1B
1C	CANC-1C
1D	CANC-1D
1E	CANC-2I
1F	CANC-1F
1G	CANC-1G
1H	CANC-1H
1I	CANC-1I
1J	
1K	CANC-1K
1L	CANC-1L
1M	
1N	CANC-1N
1P	CANC-1P
1Q	
1R	
1S	CANC-1S
1T	
1U	CANC-1U
1V	
1W	CANC-1W
1X	CANC-1X
1Y	CANC-1Y

CDM2-SIDE 2

2B	CANC-2B
2C	CANC-2C
2D	
2E	CANC-2E
2F	CANC-2F
2G	CANC-2G
2H	CANC-2H
2I	
2J	
2K	CANC-2K
2L	
2M	

CDM2-SIDE 2 (CONTINUED)

PIN	
2N	CANC-2N
2P	
2Q	
2R	CANC-2R
2S	
2T	CANC-2T
2U	
2V	CANC-2V
2W	CANC-2V
2X	CANC-2X
2Y	CANC-2Y

CDM3-SIDE 1

1B	CANC-1B
1C	CANC-1C
1D	CANC-1D
1E	CANC-2L
1F	CANC-1F
1G	CANC-1G
1H	CANC-1H
1I	CANC-1I
1J	
1K	CANC-1K
1L	CANC-1L
1M	
1N	CANC-1N
1P	CANC-1P
1Q	
1R	
1S	CANC-1S
1T	
1U	CANC-1U
1V	
1W	CANC-1W
1X	CANC-1X
1Y	CANC-1Y

CDM3-SIDE 2

2B	CANC-2B
2C	CANC-2C
2D	
2E	CANC-2E
2F	CANC-2F

CDM3-SIDE 2 (CONTINUED)

PIN	
2G	CANC-2G
2H	CANC-2H
2I	
2J	
2K	CANC-2K
2L	
2M	
2N	CANC-2N
2P	
2Q	
2R	CANC-2R
2S	
2T	CANC-2T
2U	
2V	CANC-2V
2W	CANC-2V
2X	CANC-2X
2Y	CANC-2Y

CK-SIDE 1

*	1B	TW-G, H-CMD2-1B, H-CMON-1B
*	1C	CR-1J
*	1D	TW-G, IA-1P
*	1E,2,3	C-NANC-2U, H-NANC-2U
*	1F,2,3	NANC-2S
*	1G,2,3	NANC-2Q
*	1H,2,3	A-NANC-2U, B-NANC-2U
*	1I,2,3	IC-1Y
*	1J,2,3	IC-1X
*	1K,1,2	TW-G, EH-31
	1L	
	1M,3	IH-1X
*	1N	TW-G, IB-1P
*	1P,1,2	TW-G, IH-1P
	1Q	
	1R	
	1S,3	IH-1Y
	1T	
*	1U	TW-G, B-CMD2-1B, B-CMON-1B
	1V	
*	1W	TW-G, A-CMD2-1B, A-CMON-1B
	1X	
*	1Y	TW-G, C-CMD2-1B, C-CMON-1B

CK-SIDE 2

PIN	
2B	
2C	
2D	
2E	
2F	
2G	
2H	
2I	
2J	
2K	
2L	
2M	
2N	
2P	
2Q	
2R	
2S	
2T	
2U	
2V	
2W	
2X	
2Y	

CMD1-SIDE 1

PIN	
1B	
* 1C	CCM1 & 2-1K, CMON-1C
* 1D	CCM1 & 2-1Q, CMON-1D
1E	
1F	
* 1G	CCM1 & 2-2I, CMON-1G
*A-1H	A-CCM1&2-2B,A-CMON-1H,LD-1I
*B-1H	B-CCM1&2-2B,B-CMON-1H,LD-2I
*C-1H	C-CCM1&2-2B,C-CMON-1H,LD-2C
*H-1H	H-CCM1&2-2B,H-CMON-1H,LD-1C
*A-1I	A-CCM1&2-1Y,A-CMON-1I,LA-1M
*B-1I	B-CCM1&2-1Y,B-CMON-1I,LD-2Y
*C-1I	C-CCM1&2-1Y,C-CMON-1I,LD-2S
*H-1I	H-CCM1&2-1Y,H-CMON-1I,LD-1S
1J	
* 1K	CCM1 & 2-1S, CMON-1K
1L	
1M	
* 1N	CCM1 & 2-1P, CMON-1N

CMD1-SIDE 1 (CONTINUED)

PIN	
*A-1P	A-CCM1&2-2X,A-CMON-1P,LD-1X
*B-1P	B-CCM1&2-2X,B-CMON-1P,LD-2W
*C-1P	C-CCM1&2-2X,C-CMON-1P,LD-2Q
*H-1P	H-CCM1&2-2X,H-CMON-1P,LD-1Q
*A-1Q	A-CCM1&2-1E,A-CMON-1Q,LD-1M
*B-1Q	B-CCM1&2-1E,B-CMON-1Q,LD-2M
*C-1Q	C-CCM1&2-1E,C-CMON-1Q,LD-2G
*H-1Q	H-CCM1&2-1E,H-CMON-1Q,LD-1G
*A-1R	A-CCM1&2-2H,A-CMON-1R,LD-1H
*B-1R	B-CCM1&2-2H,B-CMON-1R,LD-2H
*C-1R	C-CCM1&2-2H,C-CMON-1R,LD-2B
*H-1R	H-CCM1&2-2H,H-CMON-1R,LD-1B
1S	
* 1T	CCM1-1M & 1G, CMON-1T
1U	
1V	
1W	
*A-1X	A-CCM1&2-2Y,A-CMON-1X,LA-1N
*B-1X	B-CCM1&2-2Y,B-CMON-1X,LD-1U
*C-1X	C-CCM1&2-2Y,C-CMON-1X,LD-2T
*H-1X	H-CCM1&2-2Y,H-CMON-1X,LD-1T
1Y	

CMD1-SIDE 2

PIN	
*A-2B	A-CCM1&2-1D,A-CMON-2B,LD-1J
*B-2B	B-CCM1&2-ID,B-CMON-2B,LD-2J
*C-2B	C-CCM1&2-1D,C-CMON-2B,LD-2D
*H-2B	H-CCM1&2-1D,H-CMON-2B,LD-1D
* 2C	CCM1 & 2-2K, CMON-2C
2D	CANC-1V
* 2E	CCM1 & 2-1J, CMON-2E
2F	
* 2G	CCM1 & 2-2L, CMON-2G
2H	
2I	
2J	
*A-2K	A-CMON-2K, LA-1X
*B-2K	B-CMON-2K, LA-1Y
*C-2K	C-CMON-2K, LA-1W
*H-2K	H-CMON-2K, LA-1B
* 2L	CCM1 & 2-2P, CMON-2L
*A-2M	A-CMON-2M, LA-1T
*B-2M	B-CMON-2M, LA-1U
*C-2M	C-CMON-2M, LA-1S

CMD1-SIDE 2 (CONTINUED)

PIN	
*H-2M	H-CMON-2M,LA-1C
*A-2N	A-CCM1&2-2C,A-CMON-2N,LD-1L
*B-2N	B-CCM1&2-2C,B-CMON-2N,LD-2L
*C-2N	C-CCM1&2-2C,C-CMON-2N,LD-2F
*H-2N	H-CCM1&2-2C,H-CMON-2N,LD-1F
* 2P	CCM1&2-1R,CMON-2P
*A-2Q	A-CCM1&2-2D,A-CMON-2Q,LD-1K
*B-2Q	B-CCM1&2-2D,B-CMON-2Q,LD-2K
*C-2Q	C-CCM1&2-2D,C-CMON-2Q,LD-2E
*H-2Q	H-CCM1&2-2D,H-CMON-2Q,LD-1E
*A-2R	A-CCM1&2-2W,A-CMON-2R,LD-1Y
*B-2R	B-CCM1&2-2W,B-CMON-2R,LD-2X
*C-2R	C-CCM1&2-2W,C-CMON-2R,LD-2R
*H-2R	H-CCM1&2-2W,H-CMON-2R,LD-1R
2S	
* 2T	CCM1 & 2-2R, CMON-2T
2U	
2V	
2W	
*A-2X	A-CCM1&2-1B,A-CMON-2X,LD-1V
*B-2X	B-CCN1&2-1B,B-CMON-2X,LD-2U
*C-2X	C-CCM1&2-1B,C-CMON-2X,LD-2N
*H-2X	H-CCM1&2-1B,H-CMON-2X,LD-1N
*A-2Y	A-CCM1&2-1C,A-CMON-2Y,LD-1W
*B-2Y	B-CCM1&2-1C,B-CMON-2Y,LD-2V
*C-2Y	C-CCM1&2-1C,C-CMON-2Y,LD-2P
*H-2Y	H-CCM1&2-1C,H-CMON-2Y,LD-1P

CMD2-SIDE 1

PIN	
A-1B	CK-1W
B-1B	CK-1U
C-1B	CK-1Y
H-1B	CK-1B
1C	NANC-2P
1D	
1E	IH-2Y
1F	
1G	
1H	
1I	
1J	
1K	CANC-2S
1L	CANC-2D
1M	

CMD2-SIDE 1 (CONTINUED)

PIN	
1N	
1P	CANC-1R
1Q	
1R	
*A-1S	A-CANC-1T,LA-1K
*B-1S	B-CANC-1T,LA-1L
*C-1S	C-CANC-1T,LA-1J
*H-1S	H-CANC-1T,LA-1I
* 1T	CMON-1J
* 1U	CMON-1U
* 1V	CMON-1V
* 1W	CMON-1W
* 1X	CMON-1E
*A-1Y	A-CMON-1Y,LA-2X
*B-1Y	B-CMON-1Y,LA-2Y
*C-1Y	C-CMON-1Y,LA-2W
*H-1Y	H-CMON-1Y,LA-1D

CMD2-SIDE 2

PIN	
2B	
2C	CANC-2Q
2D	
2E	CANC-1Q
2F	
2G	
2H	
2I	
2J	
2K	
2L	
2M	
2N	
2P	
2Q	CANC-1J
2R	
2S	
* 2T	CMON-2F
2U	CANC-1M
2V	
* 2W	CMON-2W
* 2X	CMON-2H
2Y	

CMON-SIDE 1

PIN	
A-1B	A-CK-1W
B-1B	B-CK-1U
C-1B	C-CK-1Y
H-1B	H-CK-1B
1C	CMD1-1C
1D	CMD1-1D
1E	CMD2-1X
1F	
1G	CMD1-1G
1H	CMD1-1H
1I	CMD1-1I
1J	CMD2-1T
1K	CMD1-1K
1L	
1M	
1N	CMD1-1N
1P	CMD1-1P
1Q	CMD1-1Q
1R	CMD1-1R
1S	
1T	CMD1-1T
1U	CMD2-1U
1V	CMD2-1V
1W	CMD2-1W
1X	CMD1-1X
1Y	CMD2-1Y

CMON-SIDE 2

PIN	
2B	CMD1-2B
2C	CMD1-2C
2D	
2E	CMD1-2E
2F	CMD2-2T
2G	CMD1-2G
2H	CMD2-2X
2I	
2J	
2K	CMD1-2K
2L	CMD1-2L
2M	CMD1-2M
2N	CMD1-2N
2P	CMD1-2P
2Q	CMD1-2Q
2R	CMD1-2R
2S	

CMON-SIDE 2 (CONTINUED)

PIN	
2T	CMD1-2T
2U	
2V	CCM1-1H
2W	CMD2-2W
2X	CMD1-2X
2Y	CMD1-2Y

CR-SIDE 1

PIN	
1B	
1C	
1D	
1E	
1F	
1G	
1H	
1I	
1J	CK-1C
1K	
1L	
1M	
1N	
1P	
1Q	
1R	
1S	
1T	
1U	
1V	
1W	
1X	
1Y	

CR-SIDE 2

PIN	
2B	
2C	
2D	
2E	LINT-2E
2F	
2G	
2H	

CR-SIDE 2

PIN		
	2I	
	2J	
	2K	
	2L	
	2M	
*	2N	S2-2
	2P	
*	2Q	TW-G, H-LINT-1E
	2R	
	2S	
	2T	
	2U	
	2V	
	2W	
	2X	
	2Y	

EA(1-25)

PIN		
*	1	GND
*	2	GND
	3	
*	4	GND
*	5	GND
*	6	GND
	7	IA-2R
	8	
*	9	GND
	10	IA-2G
*	11	GND
*	12	GND
	13	
*	14	GND
*	15	GND
	16	IA-1T
*	17	GND
	18	
	19	IA-1F
*	20	GND
*	21	GND
	22	IA-1I
	23	
*	24	GND
	25	CABINET 2, IH-1W
	25	CABINET 3, LA-2G

EA(26-50)

PIN		
*	26	GND
*	27	GND
	28	
*	29	GND
*	30	GND
	31	IA-1H
*	32	GND
	33	
	34	CABINET 2, IH-1Y
	34	CABINET 3, LA-2H
*	35	GND
*	36	GND
*	37	GND
	38	
*	39	GND
*	40	GND
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

EB(1-25)

PIN		
*	1	GND
*	2	GND
	3	
*	4	GND
*	5	GND
*	6	GND
	7	IB-2G
	8	
*	9	GND
	10	IB-2R
*	11	GND
*	12	GND
	13	
*	14	GND
*	15	GND
	16	IB-1F

EB(1-25) (CONTINUED)

PIN	
* 17	GND
18	
19	IB-1T
* 20	GND
* 21	GND
22	IB-1H
23	
* 24	GND
25	CABINET 1, LA-2G
25	CABINET 2, IH-1V

EB(26-50)

PIN	
* 26	GND
* 27	GND
28	
* 29	GND
* 30	GND
31	IB-1I
* 32	GND
33	
34	CABINET 1, LA-2H
34	CABINET 2, IH-1X
* 35	GND
* 36	GND
* 37	GND
38	
* 39	GND
* 40	GND
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

EC(1-25)

PIN	
1	
2	
3	
4	
5	
6	IC-1R
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	IC-1G
17	
18	
19	
20	
21	
22	
23	
24	
25	

EC(26-50)

PIN	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	
36	

EC(26-50) (CONTINUED)

	PIN	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

EH(1-25)

	PIN	
*	1	CABINET 1 & 2, GND
*	2	CABINET 1 & 2, GND
	3	
*	4	CABINET 1 & 2, GND
*	5	CABINET 1 & 2, GND
*	6	CABINET 1 & 2, GND
*	6	CABINET 3, TW-G, IH-1R
	7	IH-2G
	8	
*	9	CABINET 1 & 2, GND
	10	IH-1H
*	11	CABINET 1 & 2, GND
*	12	CABINET 1 & 2, GND
	13	
*	14	CABINET 1 & 2, GND
*	15	CABINET 1 & 2, GND
*	16	CABINET 1 & 2, IH-1F
*	16	CABINET 3, TW-G, IH-1G
*	17	CABINET 1 & 2, GND
	18	
	19	IH-1S
*	20	CABINET 1 & 2, GND
*	21	CABINET 1 & 2, GND
	22	IH-1I
	23	
*	24	CABINET 1 & 2, GND
	25	IH-1T

EH(26-50)

	PIN	
*	26	CABINET 1 & 2, GND
*	27	CABINET 1 & 2, GND
	28	
*	29	CABINET 1 & 2, GND
*	30	CABINET 1 & 2, GND
	31	CK-1K
*	32	CABINET 1 & 2, GND
	33	
	34	IH-2R
*	35	CABINET 1 & 2, GND
*	36	CABINET 1 & 2, GND
*	37	CABINET 1 & 2, GND
	38	
*	39	CABINET 1 & 2, GND
*	40	CABINET 1 & 2, GND
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

IA-SIDE 1

	PIN	
	1B	A-CANC-2N
	1C	A-CANC-2F
	1D	A-CANC-1F
	1E	A-CANC-2E
*	1F	EA-19
	1G	
*	1H	EA-31
*	1I	EA-22
	1J	A-CANC-1V
	1K	A-CANC-1U
	1L	A-CANC-2T
	1M	A-CANC-1N
	1N	A-CANC-1P
	1P	CK-1D
	1Q	A-NANC-2W
	1R	

IA-SIDE 1 (CONTINUED)

	PIN	
	1S	
*	1T	EA-16
	1U	
	1V	
	1W	
	1X	
	1Y	

IA-SIDE 2

	PIN	
	2B	
	2C	
	2D	
	2E	
	2F	
*	2G	EA-10
	2H	
	2I	
	2J	
	2K	
	2L	
	2M	
	2N	
	2P	
	2Q	
*	2R	EA-7
	2S	
	2T	
	2U	
	2V	
	2W	
	2X	
	2Y	

IB-SIDE 1

	PIN	
	1B	B-CANC-2N
	1C	B-CANC-2F
	1D	B-CANC-1F
	1E	B-CANC-2E
*	IF	EB-16
	1G	

IB-SIDE 1 (CONTINUED)

	PIN	
*	1H	EB-22
*	1I	EB-31
	1J	B-CANC-1V
	1K	B-CANC-1U
	1L	B-CANC-2T
	1M	B-CANC-1N
	1N	B-CANC-1P
	1P	CK-1N
	1Q	B-NANC-2W
	1R	
	1S	
*	1T	EB-19
	1U	
	1V	
	1W	
	1X	
	1Y	

IB-SIDE 2

	PIN	
	2B	
	2C	
	2D	
	2E	
	2F	
*	2G	EB-7
	2H	
	2I	
	2J	
	2K	
	2L	
	2M	
	2N	
	2P	
	2Q	
*	2R	EB-10
	2S	
	2T	
	2U	
	2V	
	2W	
	2X	
	2Y	

IC-SIDE 1

	PIN	
	1B	C-CANC-2N
	1C	C-CANC-2F
	1D	C-CANC-1F
	1E	C-CANC-2E
	1F	
*	1G	TW-G, EC-16
	1H	
	1I	
	1J	C-CANC-1V
	1K	C-CANC-1U
	1L	C-CANC-2T
	1M	C-CANC-1N
	1N	C-CANC-1P
	1P	
	1Q	C-NANC-2W
*	1R	TW-G, EC-6
	1S	
	1T	
	1U	
	1V	
	1W	
	1X	CK-1J
	1Y	CK-1I

IC-SIDE 2

PIN	
2B	
2C	
2D	
2E	
2F	
2G	
2H	
2I	
2J	
2K	
2L	
2M	
2N	
2P	
2Q	
2R	
2S	
2T	
2U	
2V	

IC-SIDE 2 (CONTINUED)

PIN	
2W	
2X	
2Y	

IH-SIDE 1

	PIN	
	1B	H-CANC-2N
	1C	H-CANC-2F
	1D	H-CANC-1F
	1E	H-CANC-2E
	1F,1,2	EH-16
	1G	EH-16
*	1H,1,2	EH-10
*	1I,1,2	EH-22
	1J	H-CANC-1V
	1K	H-CANC-1U
	1L	H-CANC-2T
	1M	H-CANC-1N
	1N	H-CANC-1P
	1P	CK-1P
	1Q	H-NANC-2W
	1R,2	LA-2H
	1R,3	EH-6
*	1S,1,2	EH-19
*	1T,1,2	EH-25
	1U	LA-2G
*	1V,2	EB-25
*	1W,2	EA-25
*	1X,2	EB-34
*	1X,3	CK-1M
*	1Y,2	EA-34
*	1Y,3	CK-1S

IH-SIDE 2

	PIN	
	2B	
	2C	
	2D	
	2E	
	2F	
*	2G 1,2,	EH-7

IH-SIDE 2 (CONTINUED)

	PIN	
*	2H	TB1-7 (P.S.)
	2I	
	2J	
	2K,3	H-CANC-2U
*	2L	TB1-8 (P.S.)
	2M	
	2N	
	2P	
	2Q	
*	2R,1,2	EH-34
	2S	
	2T	
	2U	
	2V	
	2W	
	2X	
*	2Y,1,2	H-CMD2-1E

LA-SIDE 1

	PIN	
	1B	H-CMD1-2K
	1C	H-CMD1-2M
	1D	H-CMD2-1Y
*	1E	H-CANC-2P,H-LINT-2P,H-NMON-2M
*	1F	C-CANC-2P,C-LINT-2P,C-NMON-2M
*	1G	B-CANC-2P,B-LINT-2P,B-NMON-2M
*	1H	A-CANC-2P,A-LINT-2P,A-NMON-2M
	1I	H-CMD2-1S
	1J	C-CMD2-1S
	1K	A-CMD2-1S
	1L	B-CMD2-1S
	1M	A-CMD1-1I
	1N	A-CMD1-1X
*	1P	S8-2
*	1Q	S12-2
*	1R,2,3	S11-2
	1S	C-CMD1-2M
	1T	A-CMD1-2M
	1U	B-CMD1-2M
*	1V,2,3	S15-2
	1W	C-CMD1-2K
	1X	A-CMD1-2K
	1Y	B-CMD1-2K

LA-SIDE 2

	PIN	
*	2B	S4-2
*	2C	S7-2
*	2D	S5-2
*	2E	S6-2
*	2F	S3-2
*	2G,2	IH-1U
*	2G,3	EA-25
*	2G,1	EB-25
*	2H,2	IH-1R
*	2H,3	EA-34
*	2H,1	EB-34
*	2I	S1-1
	2J	H-CCM1-1H
	2K	C-CCM1-1H
	2L	A-CCM1-1H
	2M	B-CCM1-1H
*	2N	S9-2
*	2P	S13-2
*	2Q	S10-2
*	2R	S14-2
	2S	H-NMD1-2K
	2T	C-NMD1-2K
	2U	A-NMD1-2K
	2V	B-NMD1-2K
	2W	C-CMD2-1Y
	2X	A-CMD2-1Y
	2Y	B-CMD2-1Y

LD-SIDE 1

PIN	
1B	H-CMD1-1R
1C	H-CMD1-1H
1D	H-CMD1-2B
1E	H-CMD1-2Q
1F	H-CMD1-2N
1G	H-CMD1-1Q
1H	A-CMD1-1R
1I	A-CMD1-1H
1J	A-CMD1-2B
1K	A-CMD1-2Q
1L	A-CMD1-2N
1M	A-CMD1-1Q
1N	H-CMD1-2X
1P	H-CMD1-2Y

LD-SIDE 1 (CONTINUED)

PIN	
1Q	H-CMD1-1P
1R	H-CMD1-2R
1S	H-CMD1-1I
1T	H-CMD1-1X
1U	B-CMD1-1X
1V	A-CMD1-2X
1W	A-CMD1-2Y
1X	A-CMD1-1P
1Y	A-CMD1-2R

LD-SIDE 2

PIN	
2B	C-CMD1-1R
2C	C-CMD1-1H
2D	C-CMD1-2B
2E	C-CMD1-2Q
2F	C-CMD1-2N
2G	C-CMD1-1Q
2H	B-CMD1-1R
2I	B-CMD1-1H
2J	B-CMD1-2B
2K	B-CMD1-2Q
2L	B-CMD1-2N
2M	B-CMD1-1Q
2N	C-CMD1-2X
2P	C-CMD1-2Y
2Q	C-CMD1-1P
2P	C-CMD1-2R
2S	C-CMD1-1I
2T	C-CMD1-1X
2U	B-CMD1-2X
2V	B-CMD1-2Y
2W	B-CMD1-1P
2X	B-CMD1-2R
2Y	B-CMD1-1I

LINT-SIDE 1

PIN	
1B	
1C	
1D	

LINT-SIDE 1 (CONTINUED)

PIN	
A-1E	H-LINT-2E
B-1E	A-LINT-2E
C-1E	B-LINT-2E
H-1E	CR-2Q
1F	NANC-1T
1G	CANC-2M
1H	NANC-1E
1I	NANC-2L
1J	
1K	
1L	
1M	
1N	
1P	
1Q	NANC-1G
1R	
1S	
1T	
1U	
1V	NMON-1L
1W	
1X	NANC-1Q
1Y	NANC-1V

LINT-SIDE 2

PIN	
2B	NANC-2G
2C	NANC-2D
2D	
*A-2E	TW-G, B-LINT-1E
*B-2E,1	TW-G, CR-2E
*B-2E,2,3	TW-G, C-LINT-1E
*C-2E,2,3	TW-G, CR-2E
*H-2E	TW-G, A-LINT-1E
2F	NANC-1M
2G	NANC-2I
2H	
2I	
2J	
2K	
2L	
2M	
2N	NANC-1J
A-2P	LA-1H

LINT-SIDE 2 (CONTINUED)

PIN	
B-2P	LA-1G
C-2P	LA-1F
H-2P	LA-1E
2Q	
2R	
2S	
2T	NMD2-1B
2U	
2V	
2W	
2X	
2Y	

NANC-SIDE 1

PIN	
* 1B	NDMO-1B
* 1C	NDMO-1C
* 1D	NDMO-1D
* 1E	LINT-1H
* 1F	NDMO-1F
* 1G	LINT-1Q
* 1H	NDMO-1H
* 1I	NDMO-1I
* 1J	LINT-2N
* 1K	NDMO-1K
* 1L	NDMO-1L
* 1M	LINT-2F
* 1N	NDMO-1N
* 1P	NDMO-1P
* 1Q	LINT-1X
* 1R	NMD2-1S
* 1S	NDMO-1S
* 1T	LINT-1F
* 1U	NDMO-1U
* 1V	LINT-1Y
* 1W	NDMO-1W
* 1X	NDMO-1X
* 1Y	NDMO-1Y

NANC-SIDE 2

PIN	
* 2B	NDMO-2B

NANC-SIDE 2 (CONTINUED)

PIN	
* 2C	NDMO-2C
* 2D	LINT-2C
* 2E	NDMO-2E
* 2F	NDMO-2F
* 2G	LINT-2B
* 2H	NDMO-2H
* 2I	LINT-2G
* 2J	NMD2-1C
* 2K	NDMO-2K
* 2L	LINT-1I
* 2M	NMD2-1G
* 2N	NDMO-2N
* 2P	CMD2-1C
2Q	CK-1G
* 2R	NDMO-2R
2S	CK-1F
* 2T	NDMO-2T
A-2U	CK-1H
B-2U	CK-1H
C-2U	CK-1E
H-2U	CK-1E
* 2V	NDMO-2V & 2W
*A-2W	IA-1Q
*B-2W	IB-1Q
*C-2W	IC-1Q
*H-2W	IH-1Q
* 2X	NDMO-2X
* 2Y	NDMO-2Y

NDMO-SIDE 1

PIN	
1B	NANC-1B
1C	NANC-1C
1D	NANC-1D
* 1E	VCC
1F	NANC-1F
* 1G	GND
1H	NANC-1H
1I	NANC-1I
1J	
1K	NANC-1K
1L	NANC-1L
1M	
1N	NANC-1N
1P	NANC-1P
1Q	

NDMO-SIDE 1 (CONTINUED)

PIN	
1R	
1S	NANC-1S
1T	
1U	NANC-1U
1V	
1W	NANC-1W
1X	NANC-1X
1Y	NANC-1Y

NDMO-SIDE 2

PIN	
2B	NANC-2B
2C	NANC-2C
2D	
2E	NANC-2E
2F	NANC-2F
* 2G	GND
2H	NANC-2H
2I	
2J	
2K	NANC-2K
2L	
2M	
2N	NANC-2N
2P	
2Q	
2R	NANC-2R
2S	
2T	NANC-2T
2U	
2V	NANC-2V
2W	NANC-2V
2X	NANC-2X
2Y	NANC-2Y

NMD1-SIDE 1

PIN	
1B	
* 1C	NMON-1C
* 1D	NMON-1D
1E	

NMD1-SIDE 1 (CONTINUED)

PIN	
1F	
* 1G	NMON-1G
* 1H	NMON-1H
* 1I	NMON-1I
1J	
* 1K	NMON-1K
1L	
1M	
* 1N	NMON-1N
* 1P	NMON-1P
* 1Q	NMON-1Q
* 1R	NMON-1R
1S	
* 1T	NMON-1T
1U	
1V	
1W	
* 1X	NMON-1X
1Y	

NMD1-SIDE 2

PIN	
* 2B	NMON-2B
* 2C	NMON-2C
2D	
* 2E	NMON-2E
2F	
* 2G	NMON-2G
2H	
2I	
2J	
*A-2K	LA-2U, A-NMON-2K
*B-2K	LA-2V, B-NMON-2K
*C-2K	LA-2T, C-NMON-2K
*H-2K	LA-2S, H-NMON-2K
* 2L	NMON-2L
2M	
* 2N	NMON-2N
* 2P	NMON-2P
* 2Q	NMON-2Q
* 2R	NMON-2R
2S	
* 2T	NMON-2T
2U	
2V	

NMD1-SIDE 2 (CONTINUED)

	PIN	
	2W	
*	2X	NMON-2X
*	2Y	NMON-2Y

NMD2-SIDE 1

	PIN	
*	1B	NMON-1B, LINT-2T
	1C	NANC-2J
	1D	
	1E	
	1F	
	1G	NANC-2M
	1H	
	1I	
	1J	
	1K	
	1L	
	1M	
	1N	
	1P	
	1Q	
	1R	
	1S	NANC-1R
*	1T	NMON-1J
*	1U	NMON-1U
*	1V	NMON-1V
*	1W	NMON-1W
*	1X	NMON-1E
*	1Y	NMON-1Y

NMD2-SIDE 2

	PIN	
	2B	
	2C	
	2D	
	2E	
	2F	
	2G	
	2H	
	2I	
	2J	

NMD2-SIDE 2 (CONTINUED)

	PIN	
	2K	
	2L	
	2M	
	2N	
	2P	
	2Q	
	2R	
	2S	
*	2T	NMON-2F
	2U	
*	2V	GND
*	2W	NMON-2W
*	2X	NMON-2H
	2Y	

NMON-SIDE 1

	PIN	
	1B	NMD2-1B
	1C	NMD1-1C
	1D	NMD1-1D
	1E	NMD2-1X
	1F	
	1G	NMD1-1G
	1H	NMD1-1H
	1I	NMD1-1I
	1J	NMD2-1T
	1K	NMD1-1K
*	1L	LINT-1V
	1M	
	1N	NMD1-1N
	1P	NMD1-1P
	1Q	NMD1-1Q
	1R	NMD1-1R
	1S	
	1T	NMD1-1T
	1U	NMD2-1U
	1V	NMD2-1V
	1W	NMD2-1W
	1X	NMD1-1X
	1Y	NMD2-1Y

NMON-SIDE 2

PIN	
2B	NMD1-2B
2C	NMD1-2C
2D	
2E	NMD1-2E
2F	NMD2-2T
2G	NMD1-2G
2H	NMD2-2X
2I	
2J	
2K	NMD1-2K
2L	NMD1-2L
A-2M	LA-1H
B-2M	LA-1G

NMON-SIDE 2 (CONTINUED)

PIN	
C-2M	LA-1F
H-2M	LA-1E
2N	NMD1-2N
2P	NMD1-2P
2Q	NMD1-2Q
2R	NDM1-2R
2S	
2T	NMD1-2T
2U	
2V	
2W	NMD2-2W
2X	NMD1-2X
2Y	NMD1-2Y

SWITCH PANEL

The following are grounded: S1-3, S2-3, S3-3, S4-1, S5-1, S6-1, S7-1, S8-1, S9-1, S10-1, S11-1 (CABINETS 2 & 3 only), S12-1, S13-1, S14-1, S15-1 (CABINETS 2 & 3 only).

The following are tied to Vcc: S1-2, S3-1, S4-3, S5-3, S6-3, S7-3, S8-3, S9-3, S10-3, S11-3 (CABINETS 2 & 3 only), S12-3, S13-3, S14-3, S15-3 (CABINETS 2 & 3 only).

The following are cross-referenced back to the master reference line listed:

Master Clear	S1-1, LA-2I
Loop Reset	S2-2, CR-2N
Load Enable	S3-2, LA-2F
Load Host	S4-2, LA-2B
Load GA (Note 1)	S5-2, LA-2D
Load GB (Note 1)	S6-2, LA-2E
Load CRT	S7-2, LA-2C
Clear Host	S8-2, LA-1P
Clear GA (Note 1)	S9-2, LA-2N
Clear GB (Note 1)	S10-2, LA-2Q
Clear CRT	S11-2, LA-1R
DNEX Host	S12-2, LA-1Q
DNEX GA (Note 1)	S13-2, LA-2P
DNEX GB (Note 1)	S14-2, LA-2R
DNEX CRT	S15-2, LA-1V

NOTE 1

LABEL	CABINET 1	CABINET 2	CABINET 3
GA	G1-3	G2-1	G3-2
GB	G1-2	G2-3	G3-1

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Maintenance Manual, Exploratory Systems Control Model (ESM)		5. TYPE OF REPORT & PERIOD COVERED Final Report July 75 - April 77
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s)		8. CONTRACT OR GRANT NUMBER(s) DCA 100-75-C-0054
9. PERFORMING ORGANIZATION NAME AND ADDRESS Burroughs Corporation Federal and Special Systems Group Paoli, PA 19301		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Task 15203 P.E. 33143K
11. CONTROLLING OFFICE NAME AND ADDRESS Defense Communications Engineering Center 1860 Wiehle Avenue Reston, VA 22090		12. REPORT DATE April 77
		13. NUMBER OF PAGES 217
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Same as 11		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same as 16

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

loops, rings, System Control, Defense Communications

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This publication is the Hardware Maintenance Manual for the Exploratory Systems Control Model (ESM). It provides the information needed for maintenance of all hardware items contained in ESM cabinets numbers 1, 2, and 3. This manual was prepared by Burroughs Corporation and is submitted in accordance with the requirements of contract DCA 100-75-C-0054.